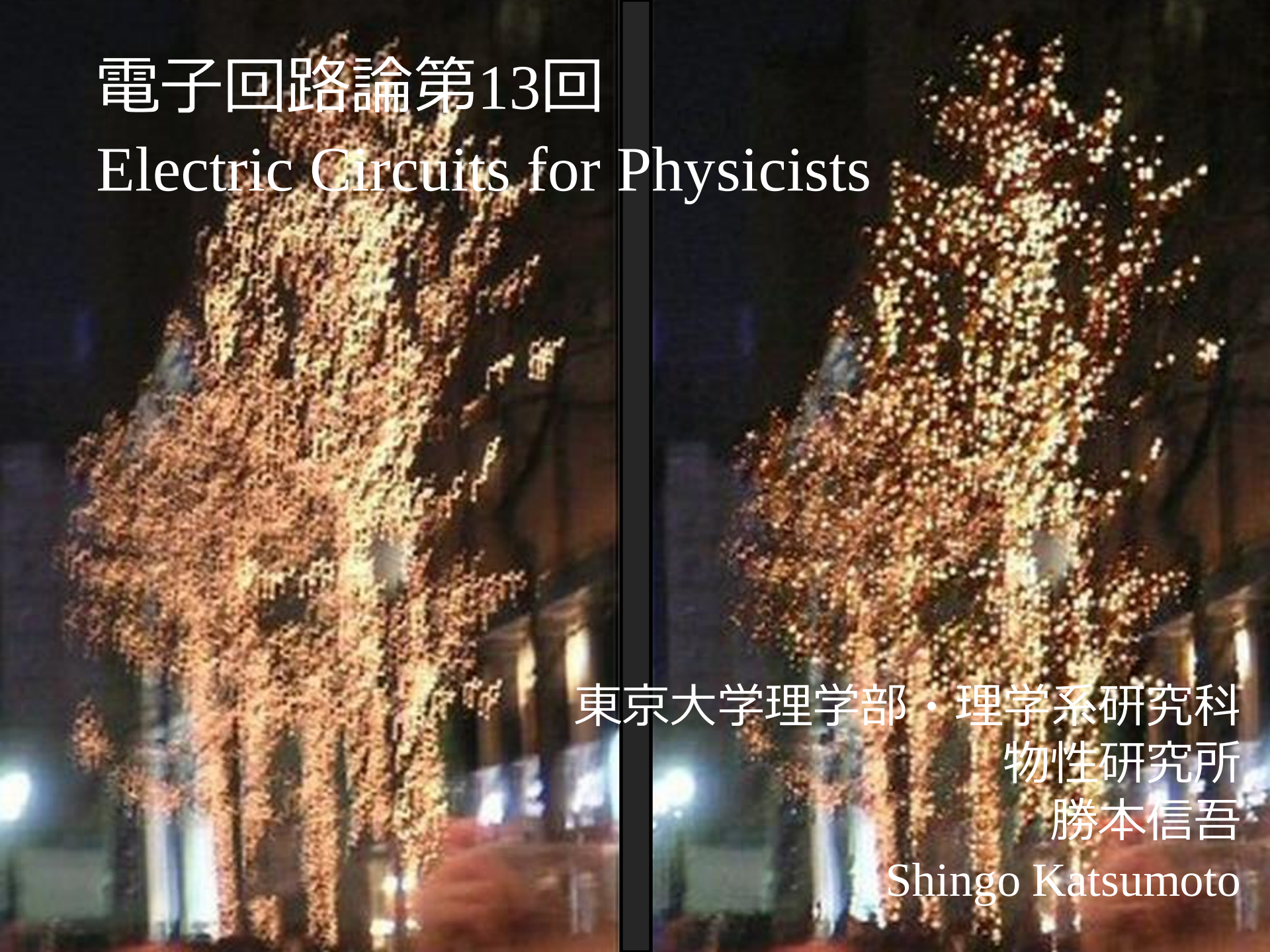
電子回路論第13回
Electric Circuits for Physicists



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勝本信吾
Shingo Katsumoto

Outline

7.2 Sequential digital circuit

7.3 Implementation of logic gates

7.4 Circuit implementation and simplification of logic operation

7.5 DA/AD converter circuits

7.6 Digital filters (digital signal processing)

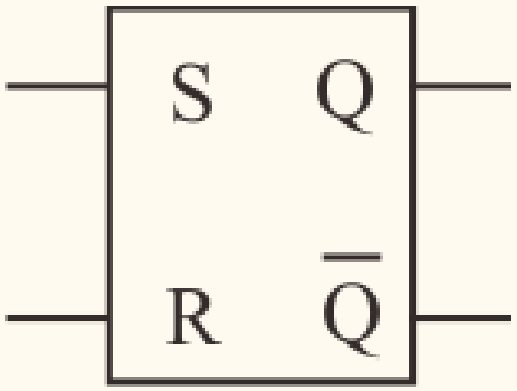
7.2.3 Sequential logic: Flip-Flop (FF)

RS (reset-set) Flip-Flop (FF)

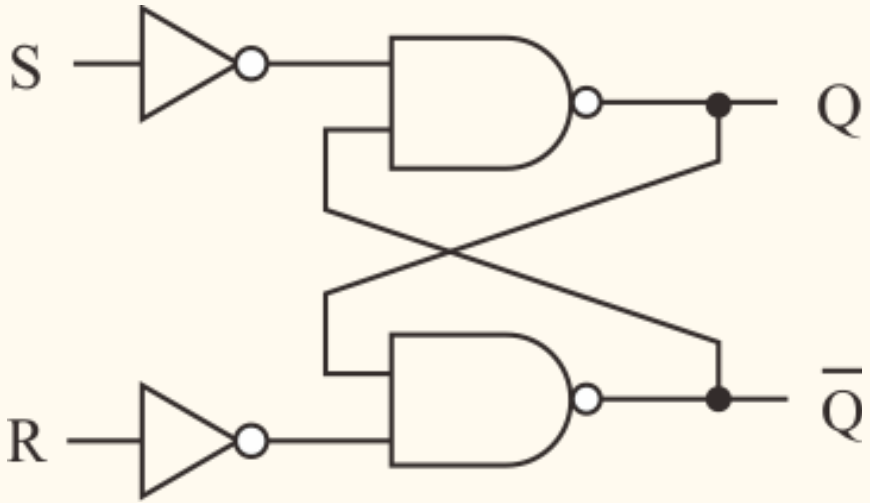
Truth table

S	R	Q	$\bar{Q}$	Response
0	0	Q	$\bar{Q}$	no change
0	1	0	1	reset
1	0	1	0	set
1	1	undetermined		

Symbol



Equivalent circuit with discrete gates



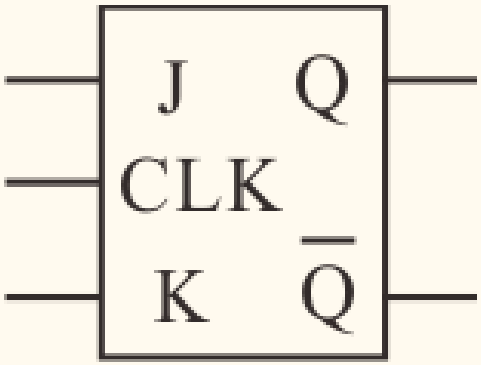
7.2.3 Sequential logic: Flip-Flop (FF)

JK Flip-Flop

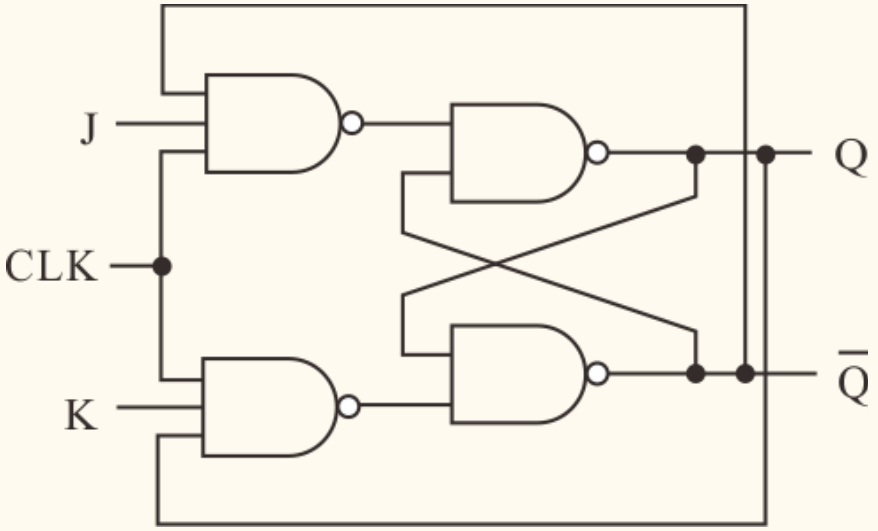
Truth table

J	K	Q	Q for the next CLK
0	0	0	0
0	0	1	1
0	1	–	0
1	0	–	1
1	1	0	1
1	1	1	0

Symbol



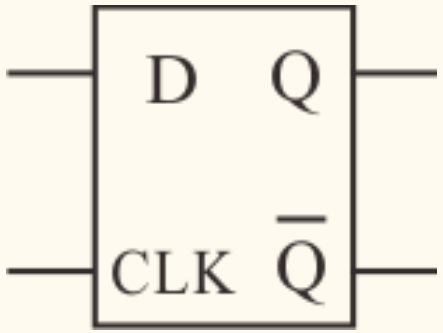
Equivalent circuit with discrete gates



7.2.3 Sequential logic: D-FF, T-FF

D-FF

Symbol

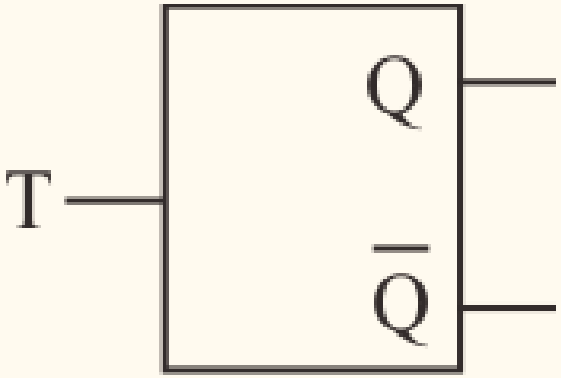


Truth table

D	CLK	Q
0	↑	0
1	↑	1
–	↓	Q (hold)

T-FF

Symbol

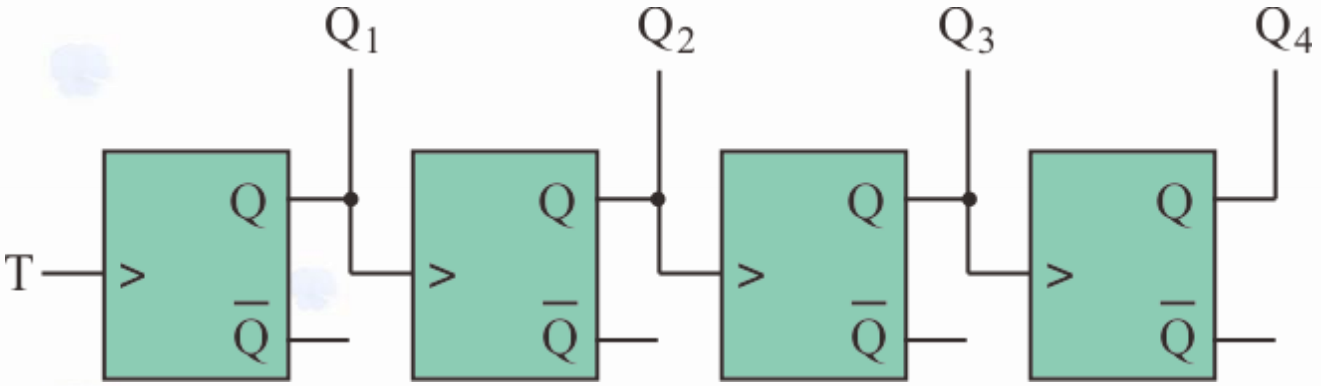


Truth table

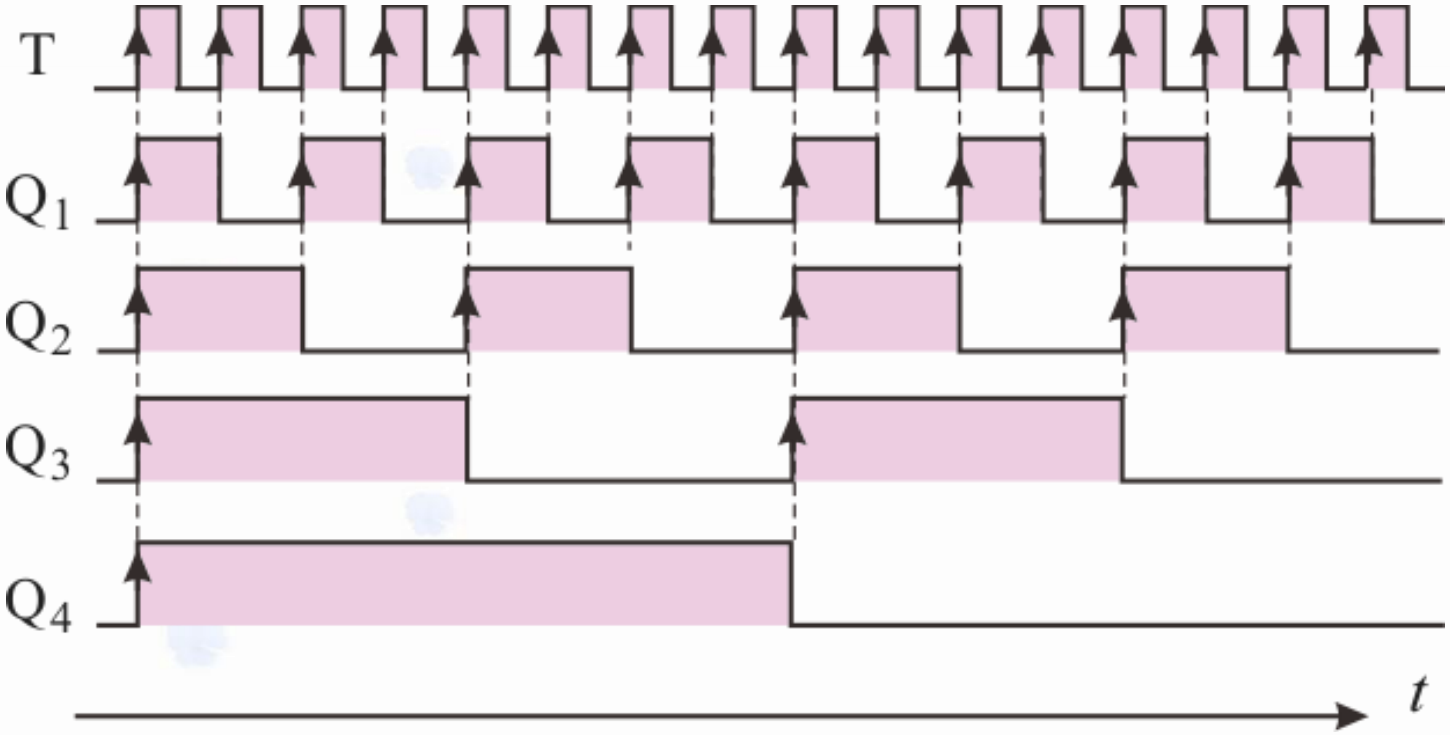
T	Q	Q
↓	0	0
↓	1	1
↑	0	1
↑	1	0

7.2.4 Sequential logic: Counters

Unsynchronized counter (ripple counter)



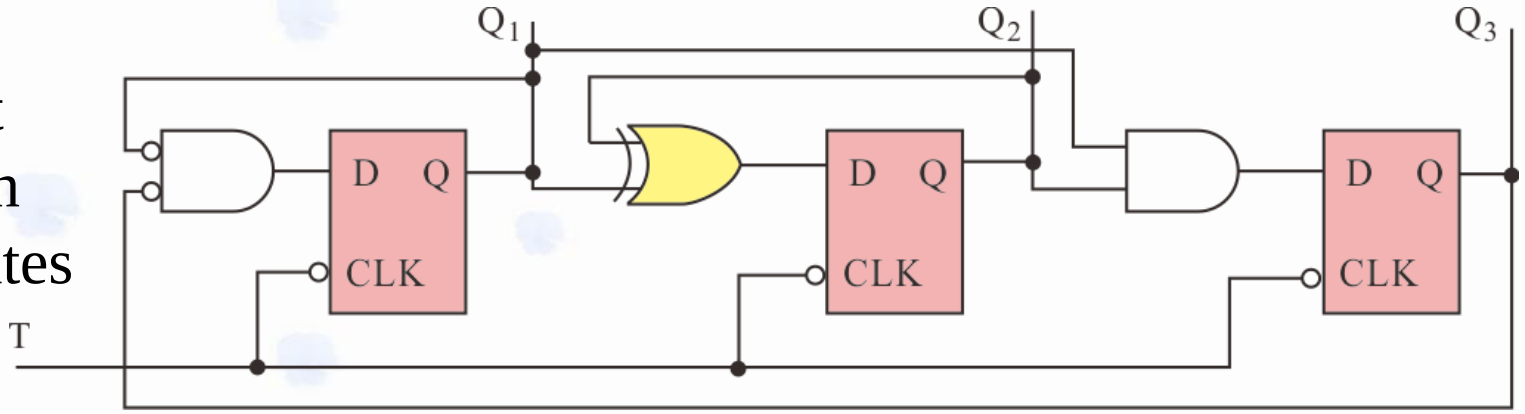
Timing chart



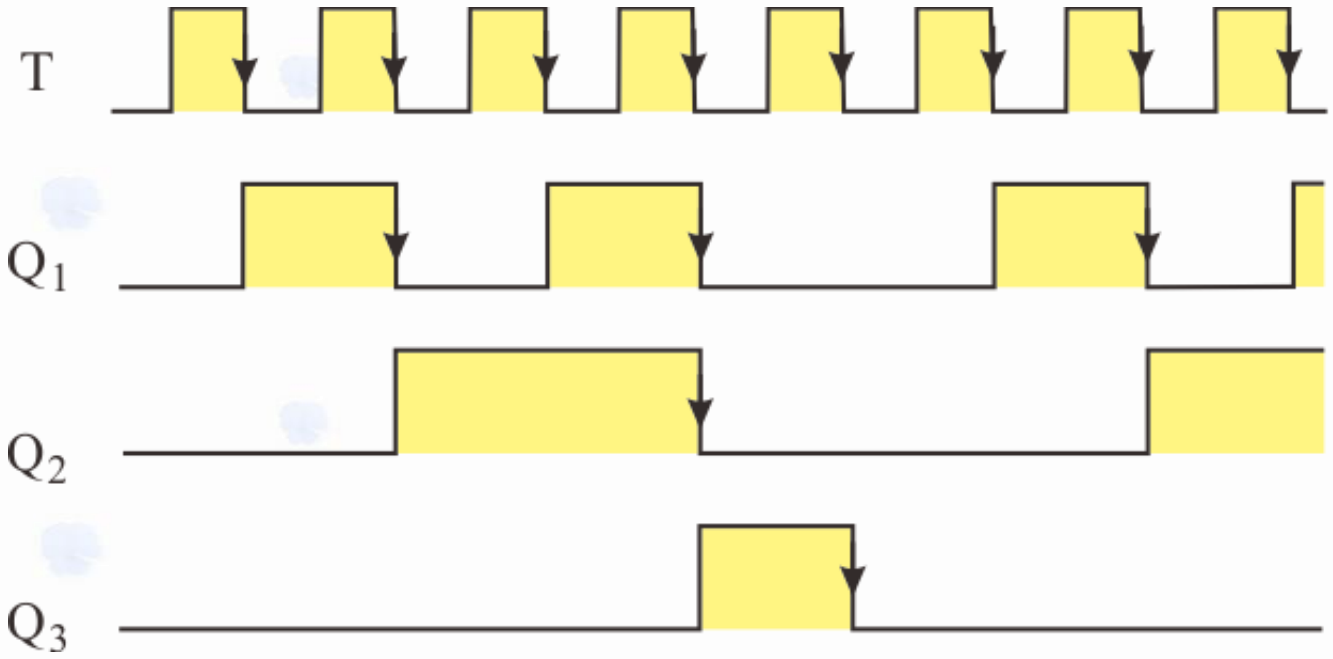
7.2.4 Sequential logic: Counters

Synchronized counter

Equivalent circuit with discrete gates



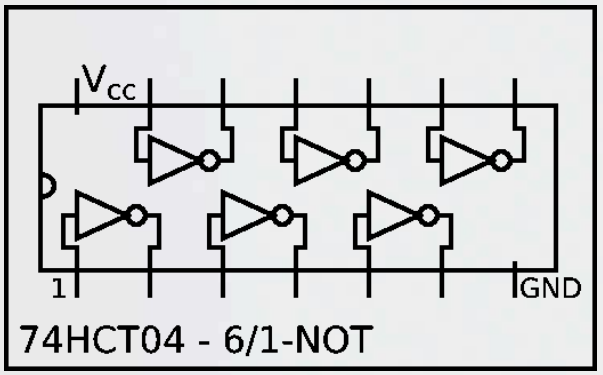
Timing chart

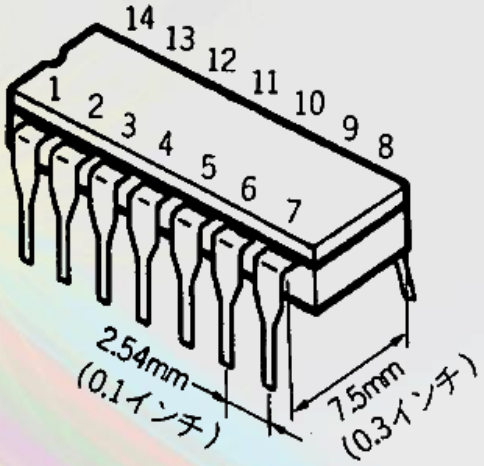


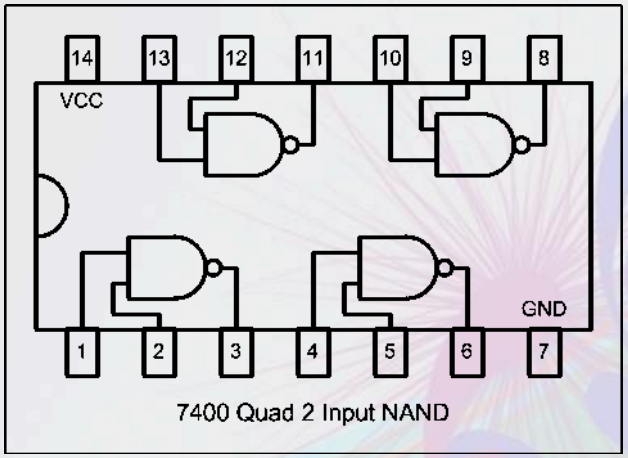
Standard gate logic IC packaging

Full pitch

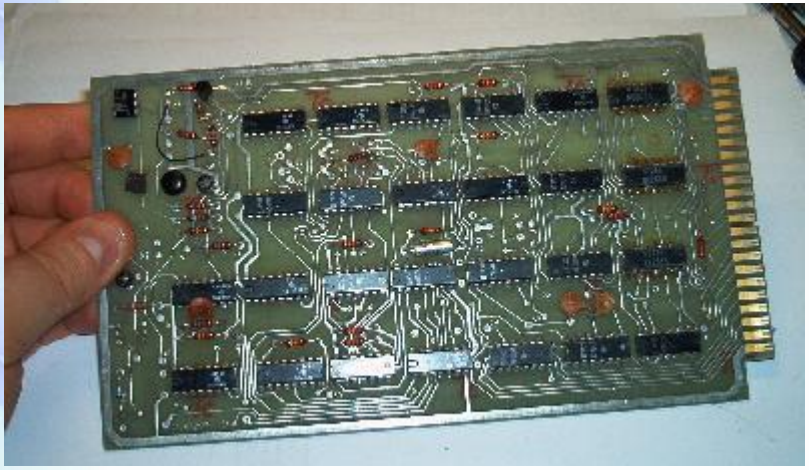
Half pitch surface mount





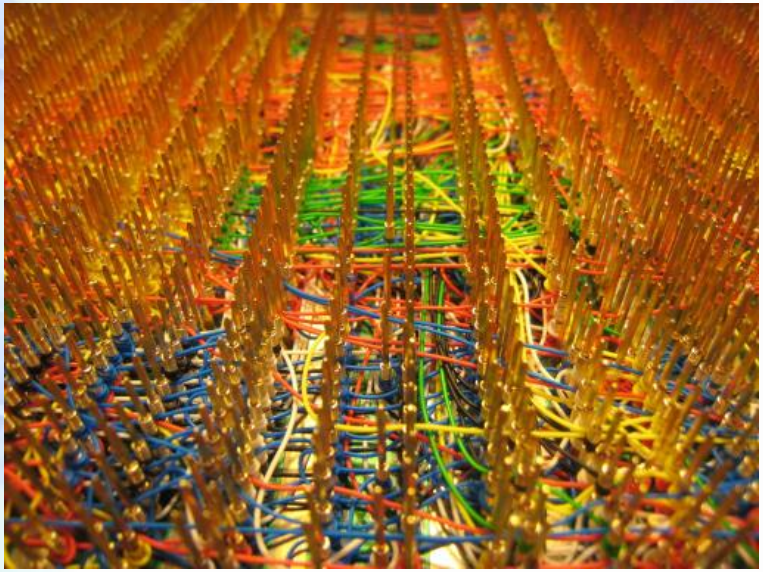


Mounting of logic ICs

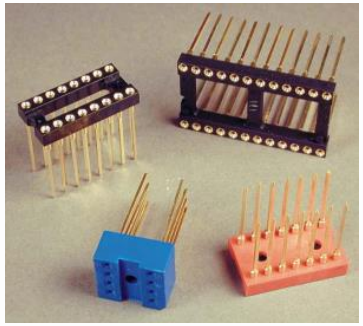


Printed board with soldering

Surface mounting

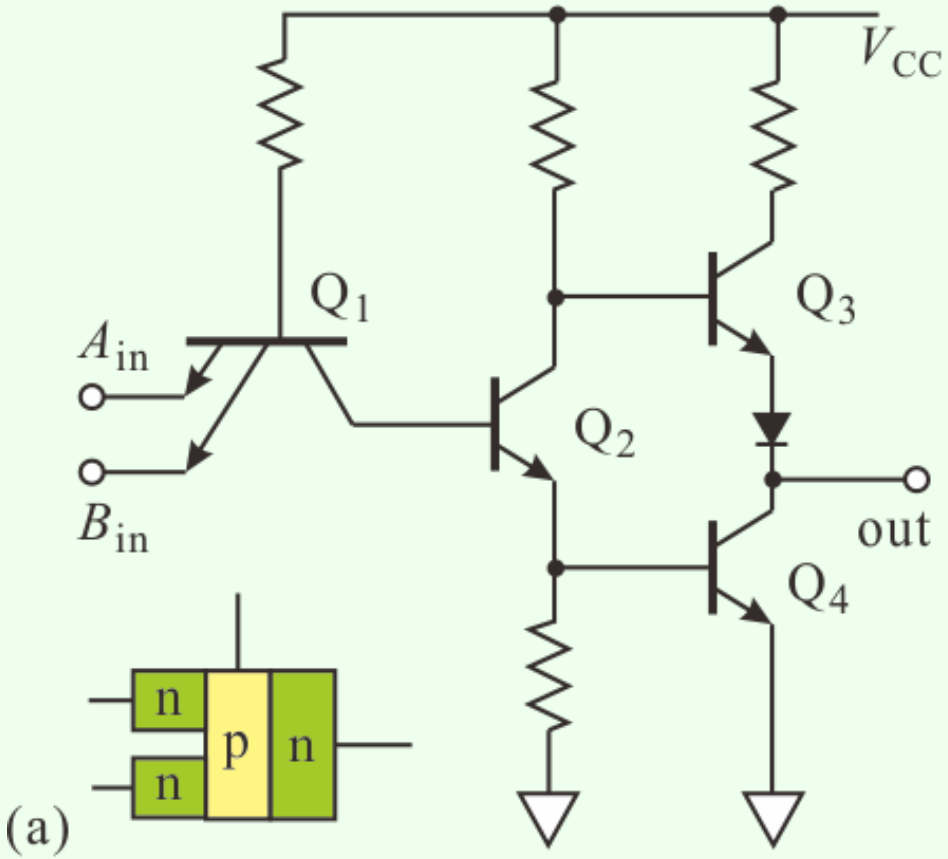


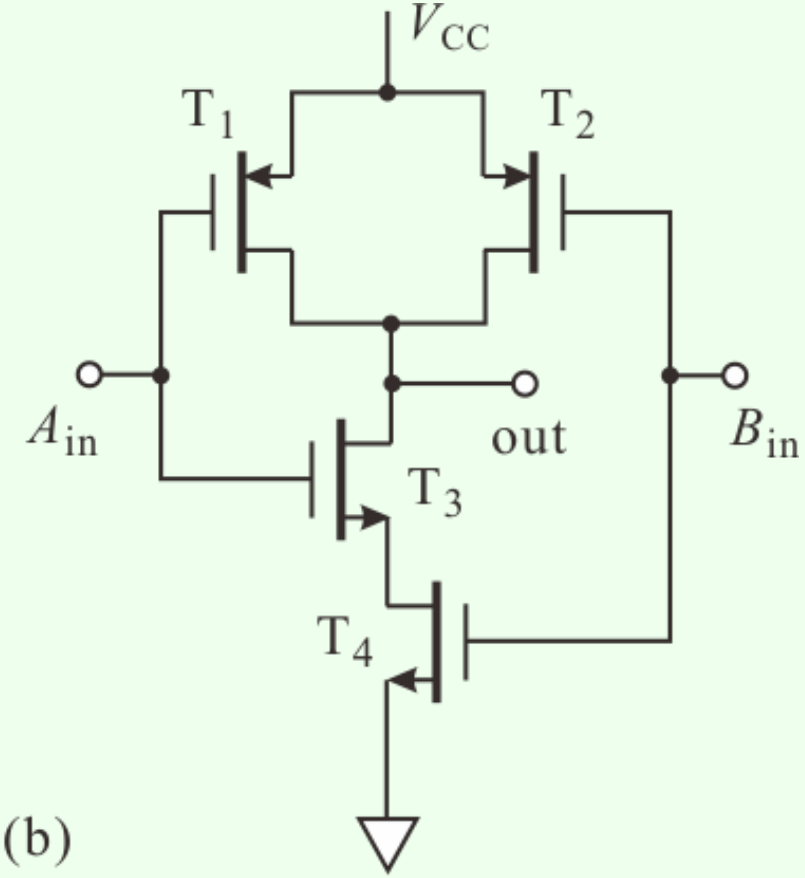
Wire wrapping



7.3 Implementation of logic gates

NAND gates



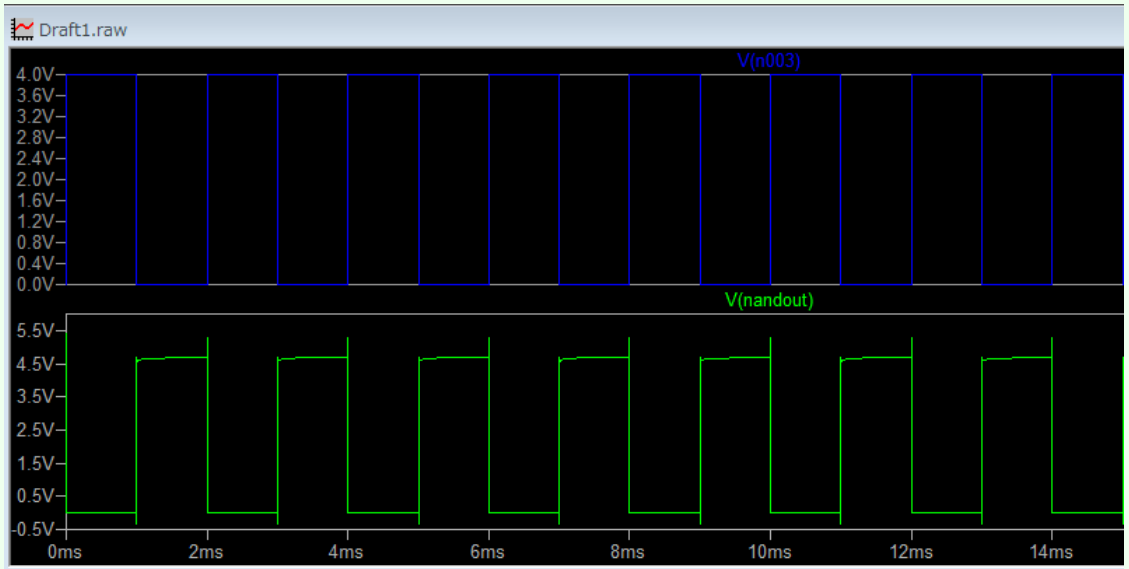


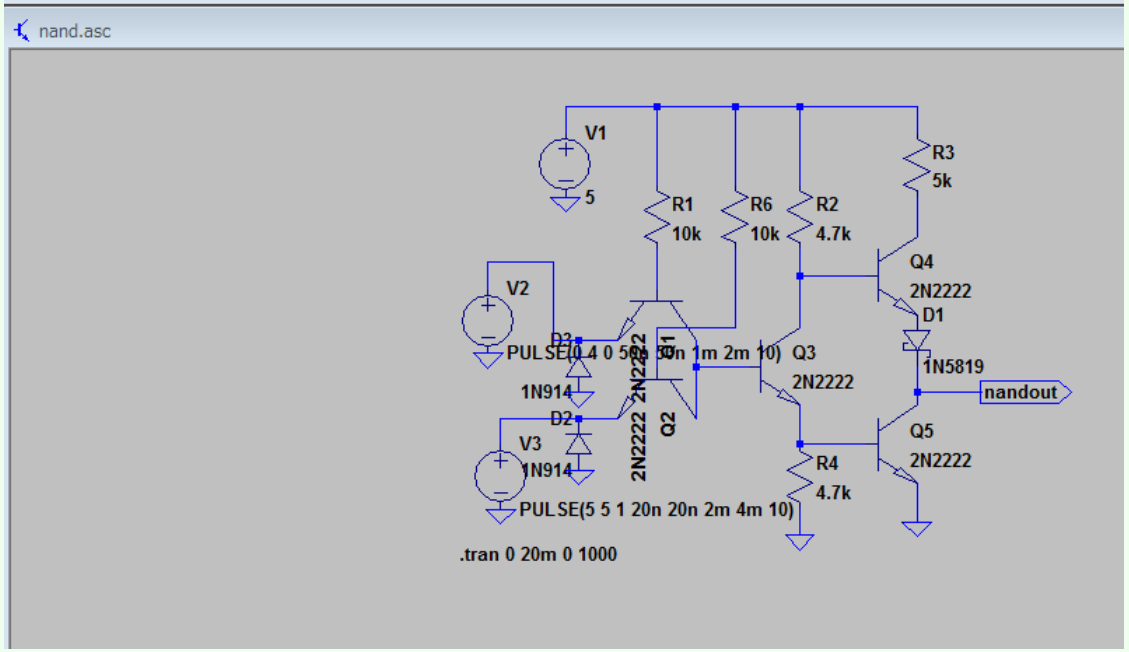
TTL (transistor-transistor logic)

CMOS (complimentary MOS)

7.3 Implementation of logic gates

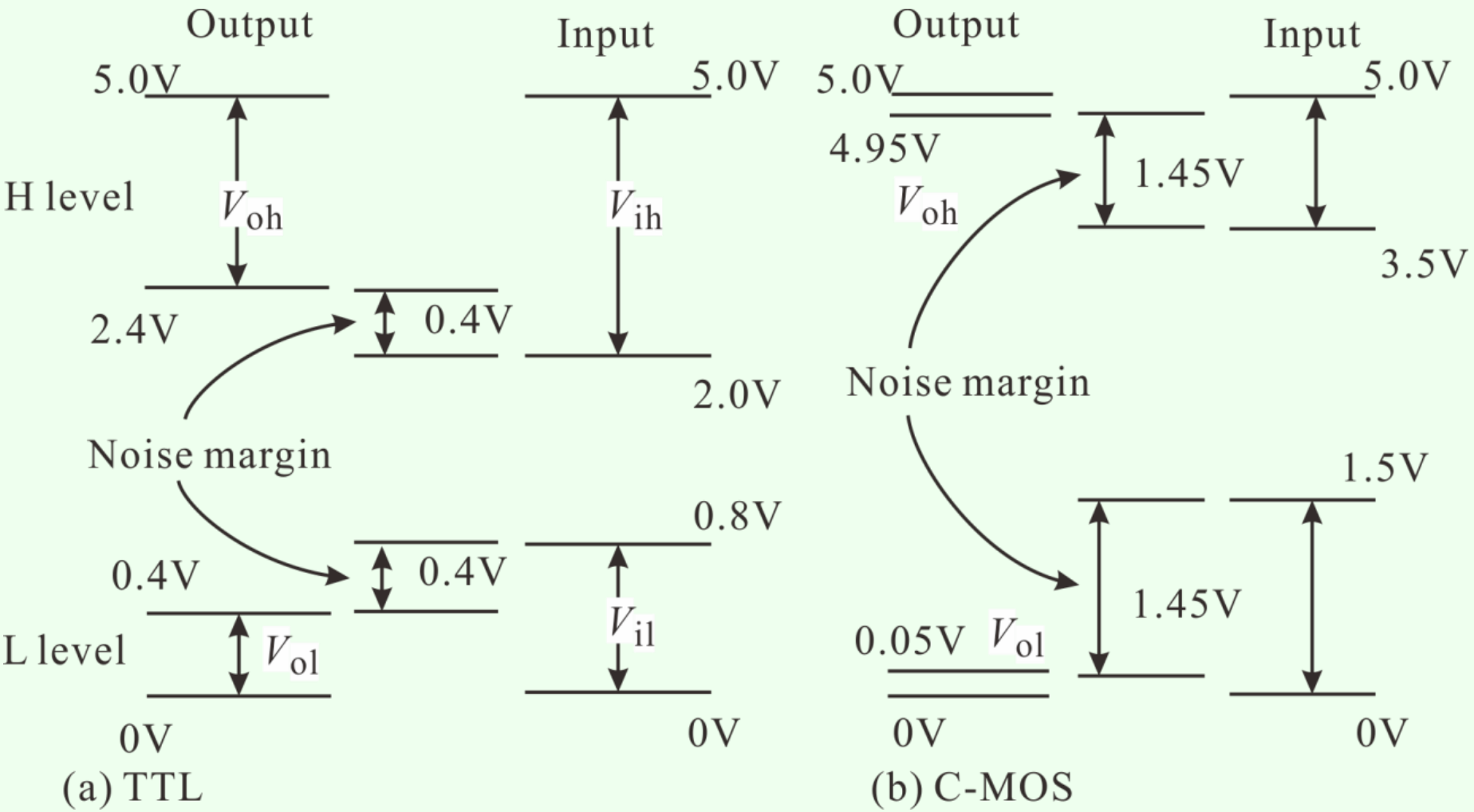
LT Spice simulation



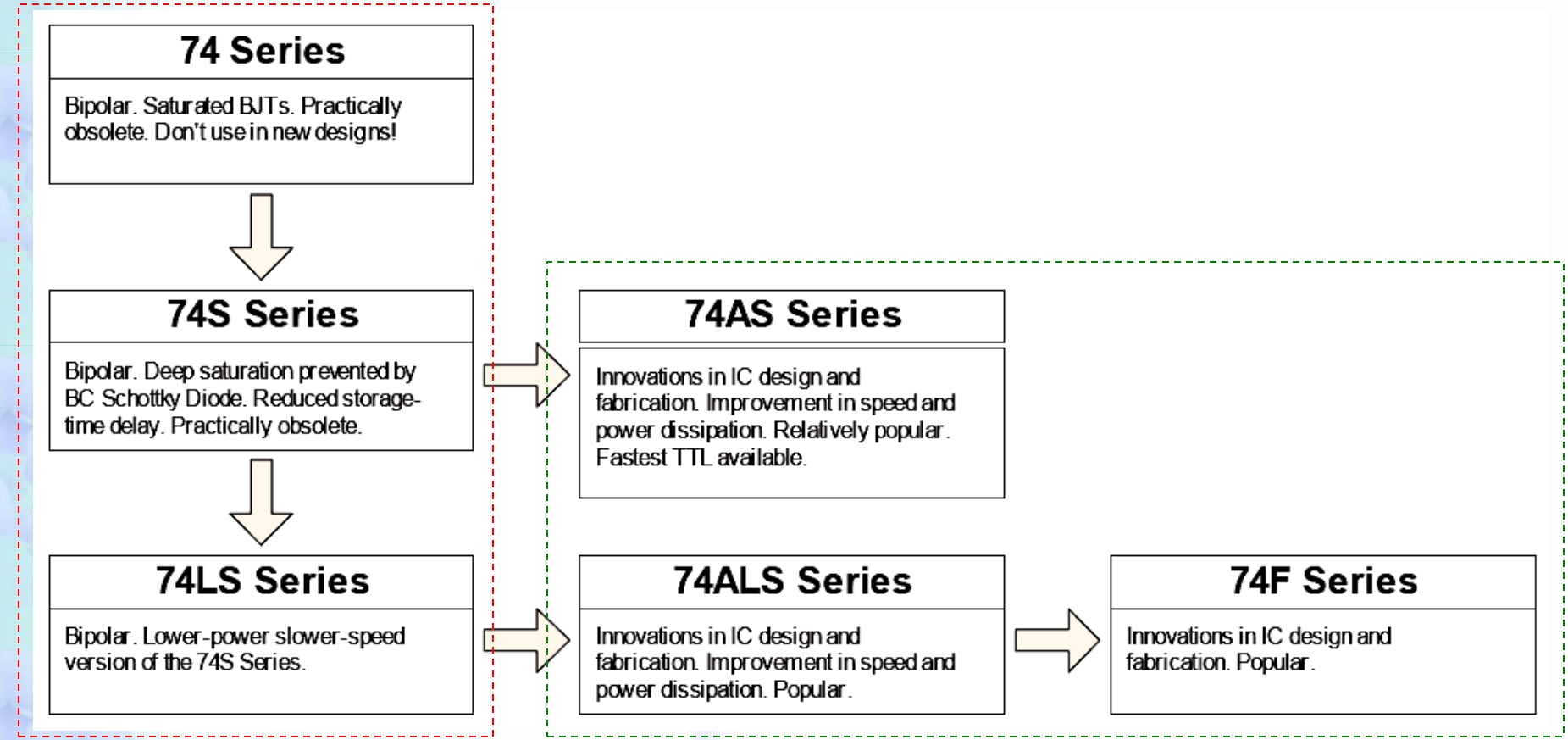


7.3 Implementation of logic gates

Voltage levels diagram



TTL logic family evolution



Legacy: don't use in new designs

Widely used today

CMOS logic family evolution

obsolete

4000 Series

CMOS. Wide supply voltage range. High noise margin. Low speed. Weak output drive. Practically obsolete.

74C Series

CMOS. Pin-compatible with TTL devices. Low speed. Obsolete. Replaced by HC/HCT family.

74HC/HCT Series

CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.

74AC/ACT Series

CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.

74AHC/AHCT Series

CMOS. Improved speed, lower power, lower drive capability.

BiCMOS Logic

CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)

74LVC/ALVC/LV/AVC

CMOS. Reduced supply voltage.
LVC: 5V/3.3V translation
ALVC: Fast 3.3V only
AVC: Optimised for 2.5V, down to 1.2V

General trend:

- Reduction of dynamic losses through successively decreasing supply voltages:
  $12V \rightarrow 5V \rightarrow 3.3V \rightarrow 2.5V \rightarrow 1.8V$
  CD4000 LVC/ALVC/AVC
- Power reduction is one of the keys to progressive growth of integration

Summary

TTL

Logic Family	T_{PD}	$T_{rise/fall}$	$V_{IH,min}$	$V_{IL,max}$	$V_{OH,min}$	$V_{OL,max}$	Noise Margin
74	22ns		2.0V	0.8V	2.4V	0.4V	0.4V
74LS	15ns		2.0V	0.8V	2.7V	0.5V	0.3V
74F	5ns	2.3ns	2.0V	0.8V	2.7V	0.5V	0.3V
74AS	4.5ns	1.5ns	2.0V	0.8V	2.7V	0.5V	0.3V
74ALS	11ns	2.3ns	2.0V	0.8V	2.5V	0.5V	0.3V
ECL	1.45ns	0.35ns	-1.165V	-1.475V	-1.025V	-1.610V	0.135V
4000	250ns	90ns	3.5V	1.5V	4.95V	0.05V	1.45V
74C	90ns		3.5V	1.5V	4.5V	0.5V	1V
74HC	18ns	3.6ns	3.5V	1.0V	4.9V	0.1V	0.9V
74HCT	23ns	3.9ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AC	9ns	1.5ns	3.5V	1.5V	4.9V	0.1V	1.4V
74ACT	9ns	1.5ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AHC	3.7ns		3.85V	1.65V	4.4V	0.44V	0.55V

CMOS

7.4 Circuit implementation and simplification of logic operation

Truth table → Simplification → Circuit diagram

Simplification
- Visual method: Karnaugh mapping
- Quine-McClusky algorithm

Product of all the logic variables: canonical expansion

principal disjunctive canonical expansion (主加法標準展開)

$$Y = \sum_{j} \prod_{i=1}^{n} g_i(a_{ij})$$

Ex) $Y = \bar{A} \cdot \bar{B} \cdot C \cdot D + B \cdot C \cdot D + A \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot C \cdot D$

$$Y = \bar{A} \cdot \bar{B} \cdot C \cdot D + (A + \bar{A}) \cdot B \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot (D + \bar{D}) + A \cdot \bar{B} \cdot C \cdot D$$
$$= \bar{A} \cdot \bar{B} \cdot C \cdot D + A \cdot B \cdot C \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot D$$
$$+ A \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot \bar{B} \cdot C \cdot D$$

Or in binary: Y = 0011+1111+0111+1101+1100+1011

Quein-McClusky algorithm

Classification with the number of 1

Num.of 1	smallest	compress1	compress2
2	0011	0_11	__11
	1100	_011	__11
3	0111	110_	
	1011	_111	
	1101	1_11	
4	1111	11_1	

Y = __11+110_+11_1 First simplification

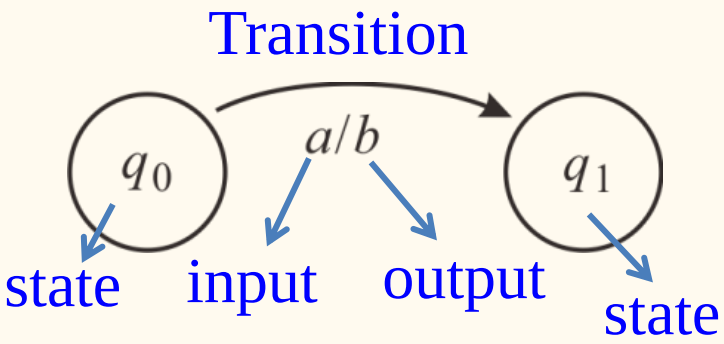
	smallest					
	0011	1100	0111	1011	1101	1111
__11	◎		◎	◎		◎
110_		◎			◎	
11_1					○	○

Y = __11+110_ Final form

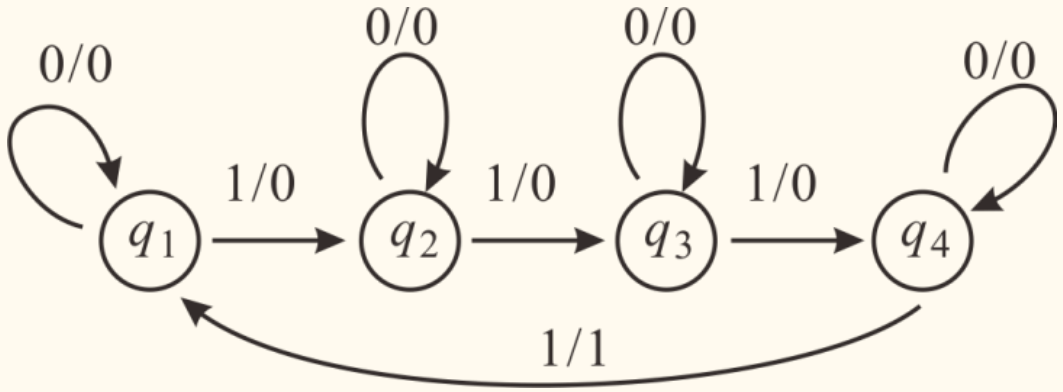
Wolfram Alpha

Design of sequential logic circuit: State diagram

State (transition) diagram:



Ex) 2-bit counter with two T-FF



FF output:

$Q_n^{(1)}, Q_n^{(2)}$

Karnaugh map simplification

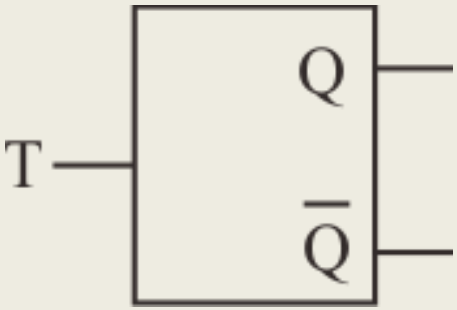
		input x					
		0			1		
		next		out	next		out
$Q_n^{(1)}$	$Q_n^{(2)}$	$Q_{n+1}^{(1)}$	$Q_{n+1}^{(2)}$	y	$Q_{n+1}^{(1)}$	$Q_{n+1}^{(2)}$	y
0	0	0	0	0	1	0	0
0	1	0	1	0	1	1	0
1	0	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Recursion equation:

$$Q_{n+1}^{(1)} = \overline{x} \cdot Q_n^{(1)} + x \cdot \overline{Q}_n^{(1)},$$

$$Q_{n+1}^{(2)} = \overline{x} \cdot Q_n^{(2)} + Q_n^{(2)} \cdot \overline{Q}_n^{(1)} + x \cdot \overline{Q}_n^{(2)} \cdot Q_n^{(1)}.$$

Design of sequential logic circuit: State diagram



T	Q	Q
↓	0	0
↓	1	1
↑	0	1
↑	1	0

Characteristic equation
(recursion equation)

$$Q_{n+1} = \alpha Q_n + \beta \overline{Q}_n$$

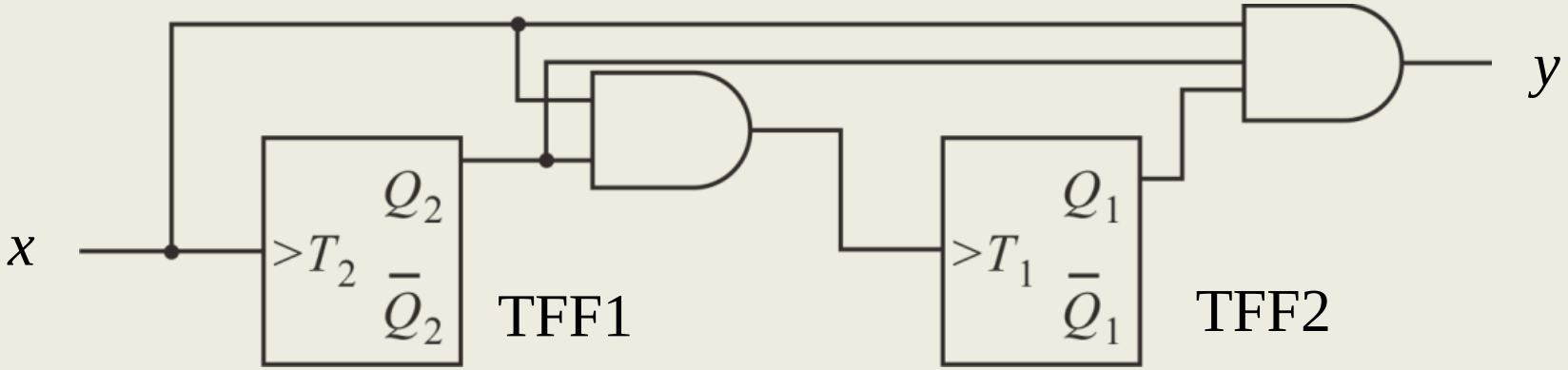
T-FF : $Q_{n+1} = \overline{T} Q_n + T \overline{Q}_n$

$$Q_{n+1}^{(1)} = \overline{x} \cdot Q_n^{(1)} + x \cdot \overline{Q}_n^{(1)},$$

$$Q_{n+1}^{(2)} = (\overline{x} + \overline{Q}_n^{(1)}) \cdot Q_n^{(2)} + (x \cdot Q_n^{(1)}) \cdot \overline{Q}_n^{(2)}$$

$$= \overline{(x \cdot Q_n^{(1)})} \cdot Q_n^{(2)} + (x \cdot Q_n^{(1)}) \cdot \overline{Q}_n^{(2)}$$

$$y = \overline{x Q_n^{(1)} Q_n^{(2)}}$$



7.5 AD/DA converter circuit

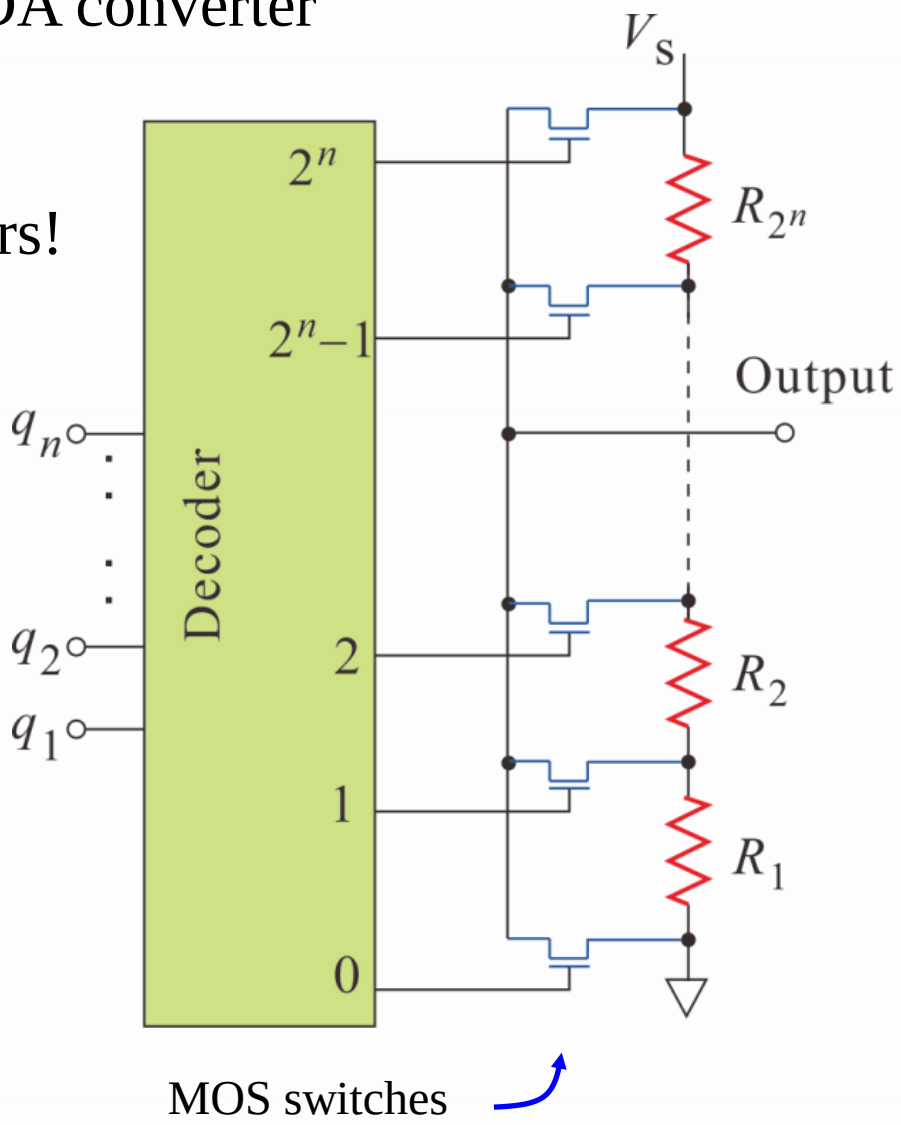
7.5.1 Digital to Analog conversion

Resistor string type DA converter

n bits converter

$\rightarrow 2^n$ outputs!, 2^n resistors!

$$V_{\text{out}} = \frac{p_{\text{input}}}{2^n} V_{\text{S}}$$

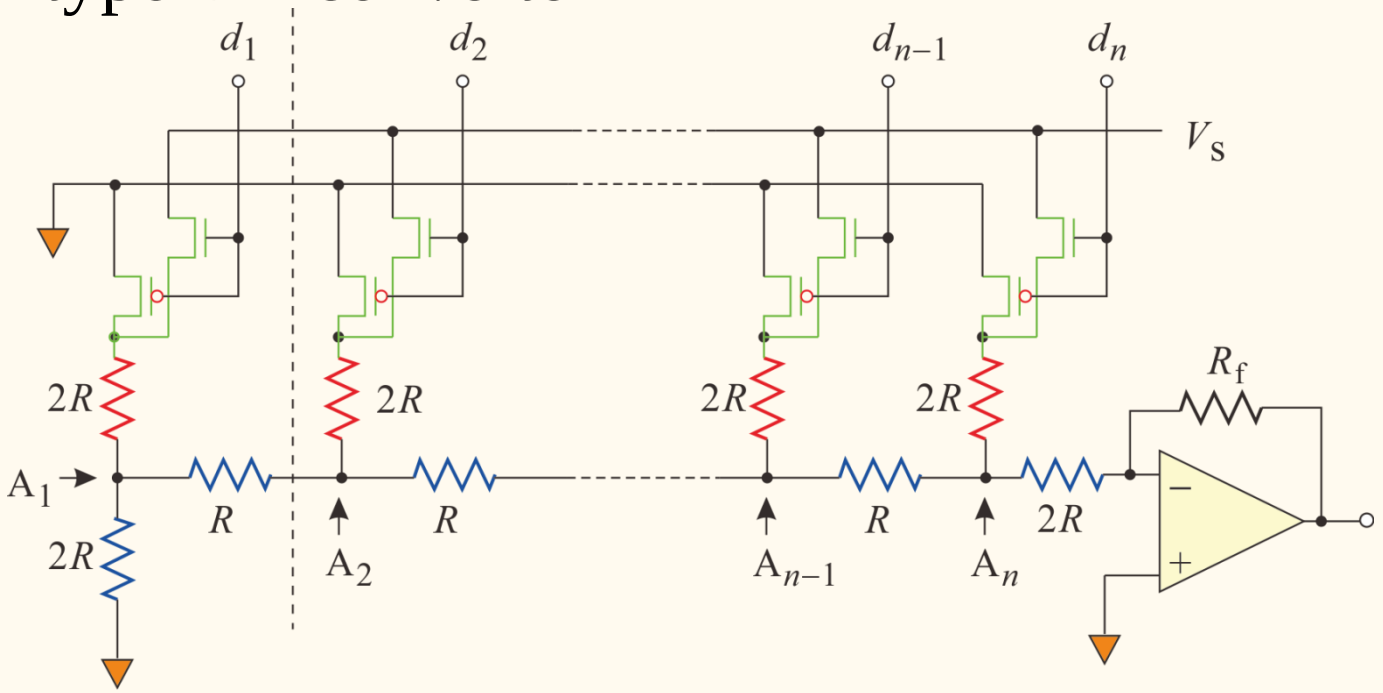


7.5.1 Digital to Analog conversion

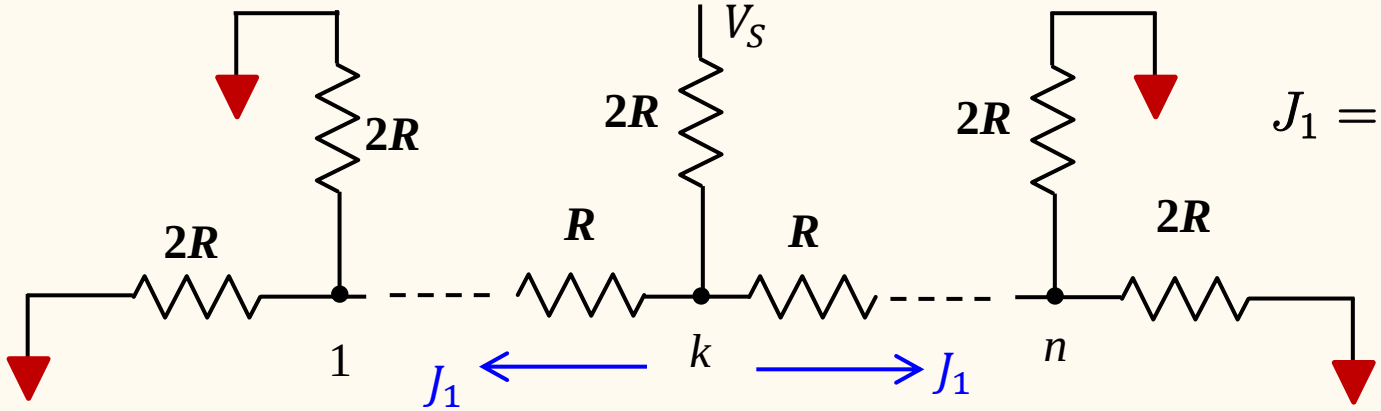
Resistor ladder type DA converter

MOS switch array

ON: V_S
OFF: ground

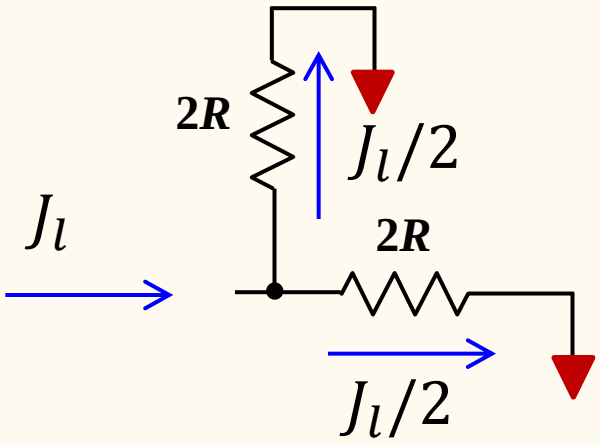


Input $(0,0,\cdots,0,1,0,\cdots,0)$ $\quad d_k = 1$, others = 0

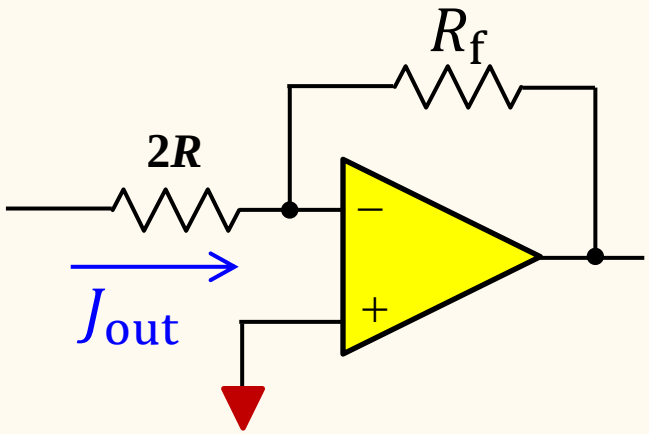


$$J_1 = \frac{V_S}{2 \cdot (2R + R)} = \frac{V_S}{6R}$$

7.5.1 Digital to Analog conversion



$$J_{l+1} = \frac{J_l}{2}$$



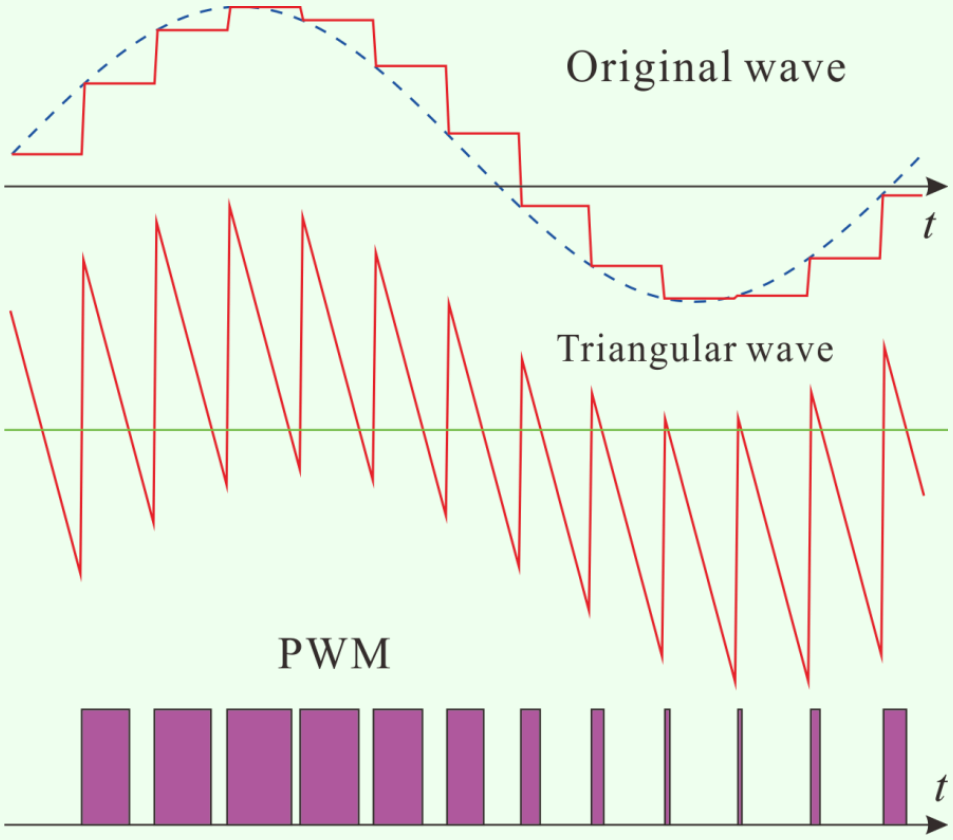
$$J_{\text{out}}(\underset{n}{0\cdots0}\ \underset{k}{1}\ \underset{1}{0\cdots0}) = \frac{V_S}{3R}\left(\frac{1}{2}\right)^{n-k+1} = \frac{V_S}{6\cdot 2^n R}2^k$$

From the superposition theorem:

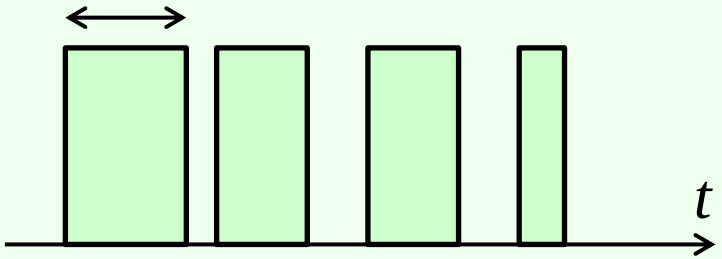
$$V_{\text{out}}(\{d_i\}) = -\frac{1}{3\cdot 2^n}\frac{R_f}{2R}V_S\sum_{k=1}^{n}2^k d_k$$

7.5.1 Digital to Analog converter

Pulse width modulation (PWM)

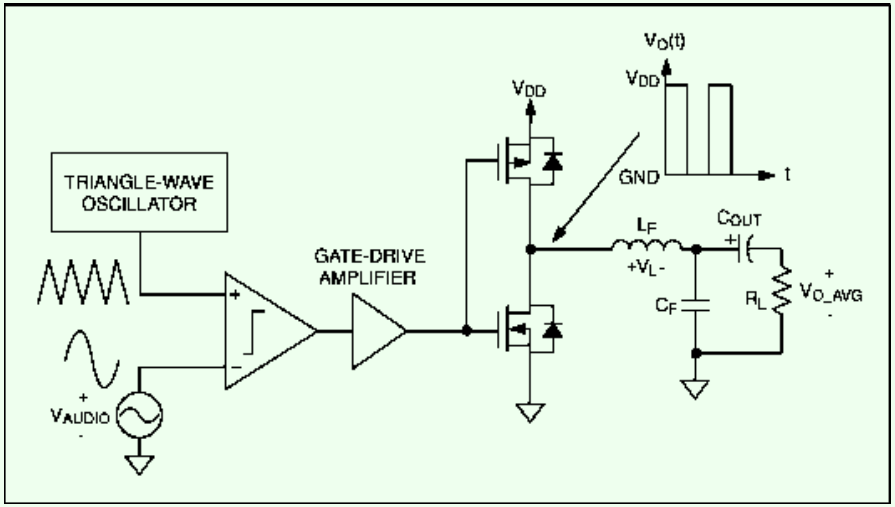


Digital signal →
PWM signal with a counter



Low pass

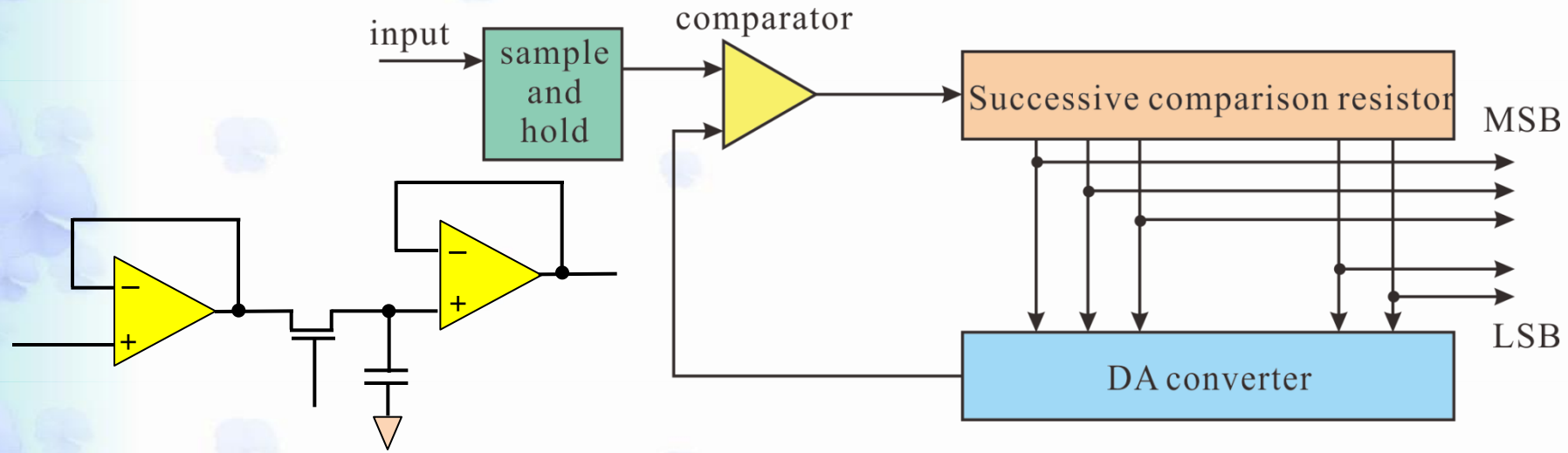
Analog signal



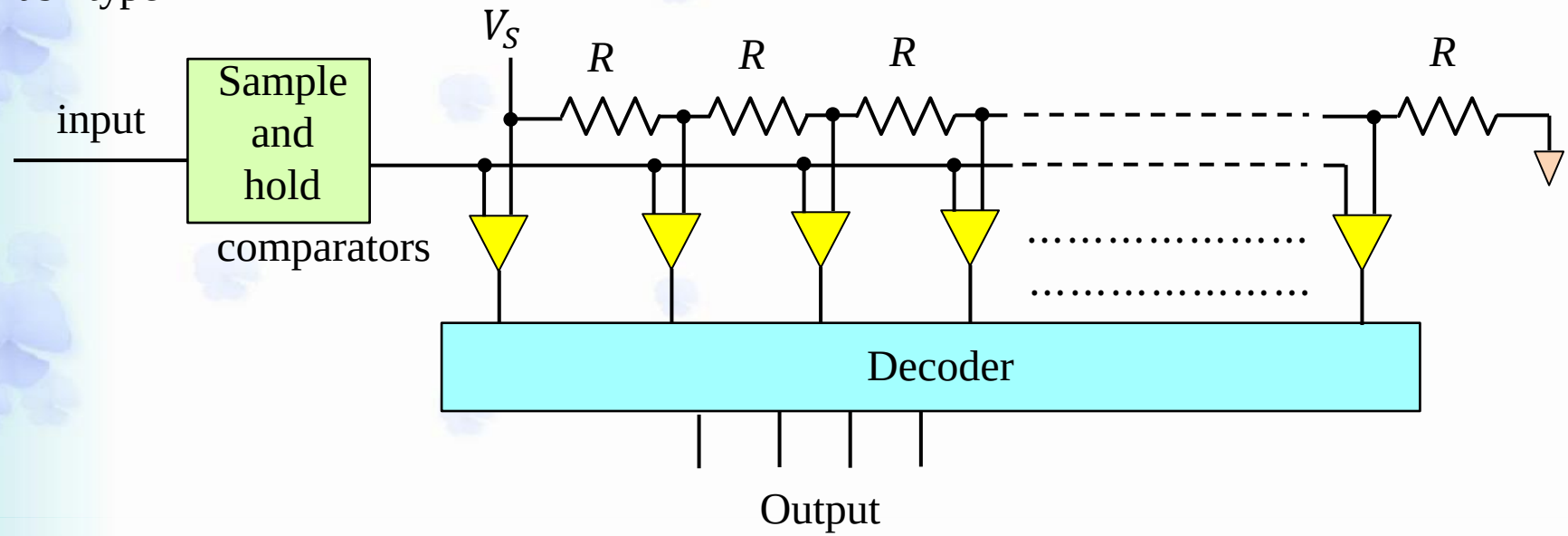
D-class amplifier

7.5.2 Analog-Digital converter

Successive comparison type AD converter

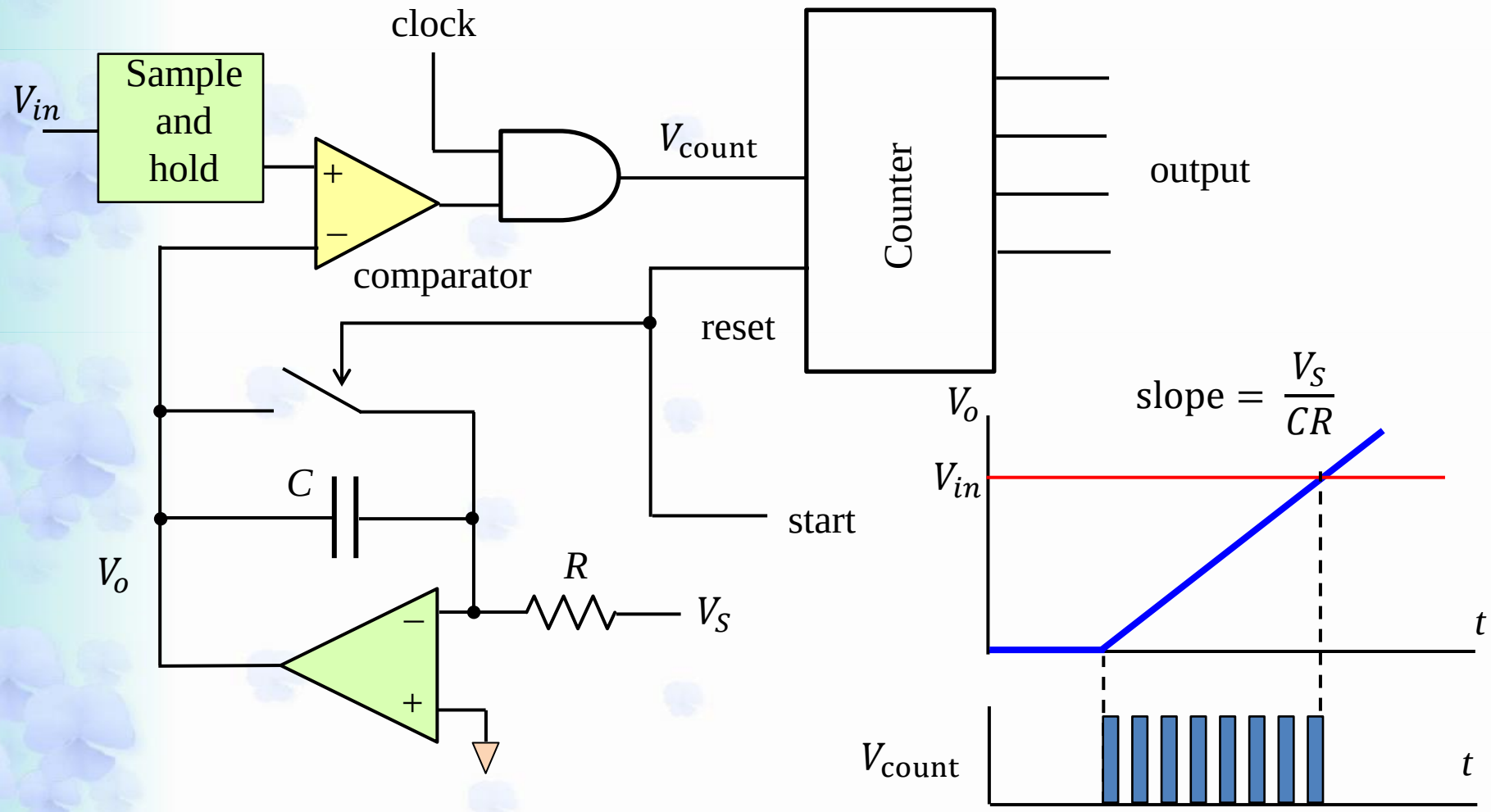


Flush type

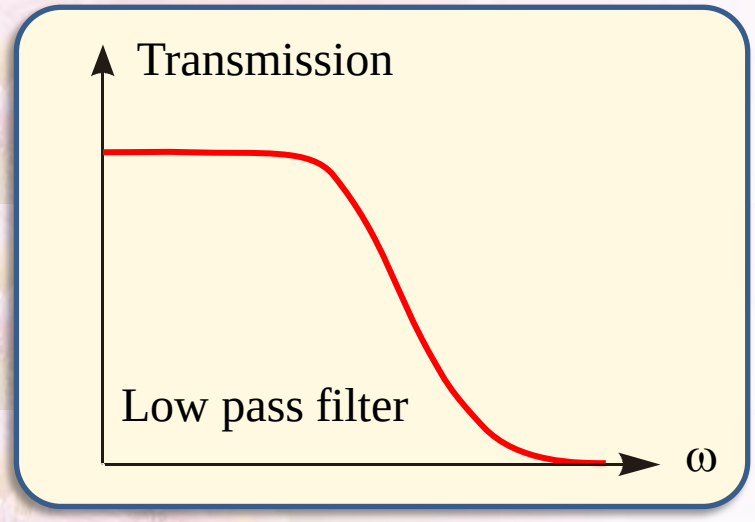


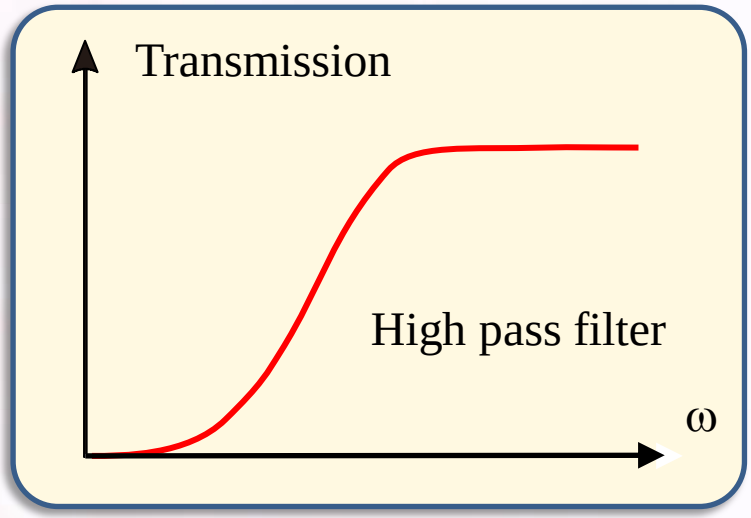
7.5.2 Analog-Digital converter

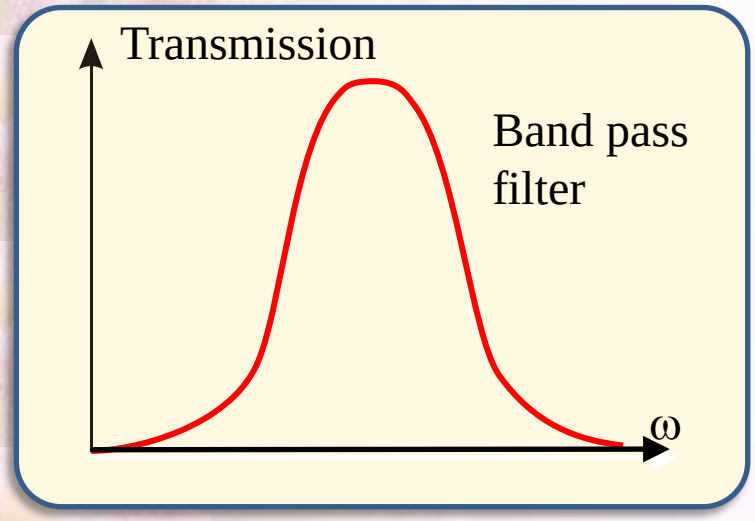
Integrating Analog-Digital Converter

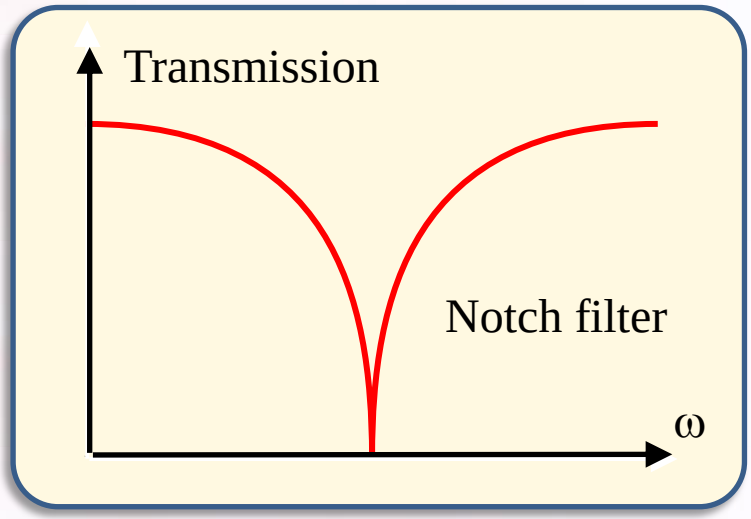


Filter Circuit



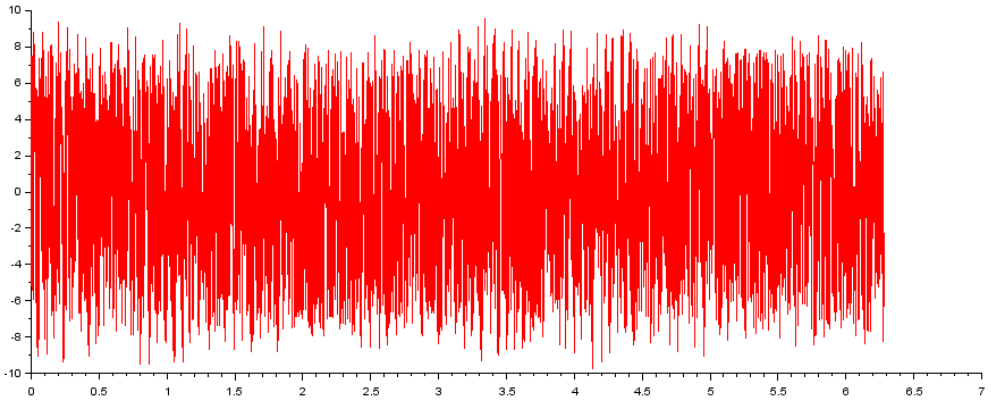




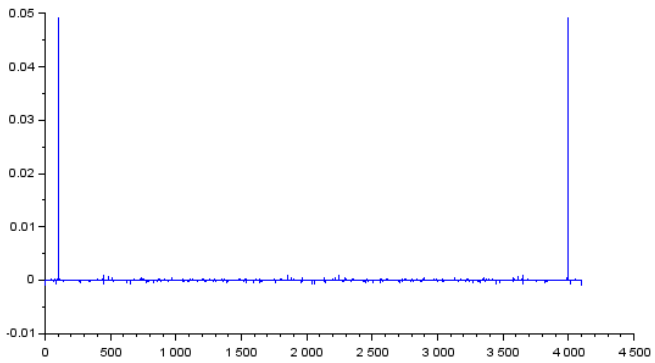


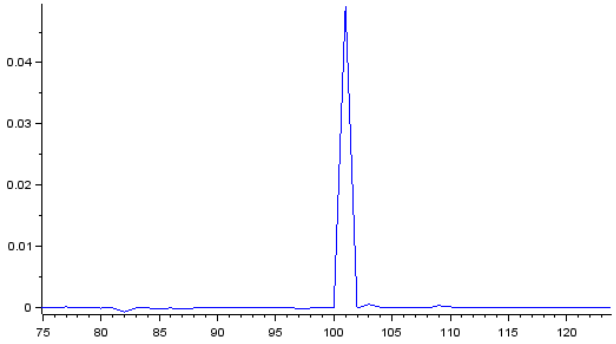
An example for retrieving data from noise

Signal with noise



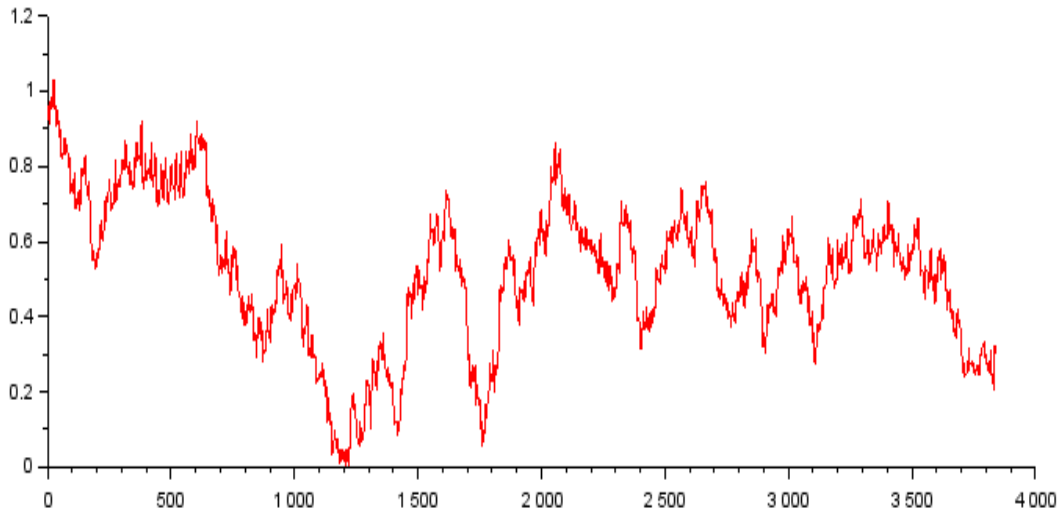
Detection of carrier



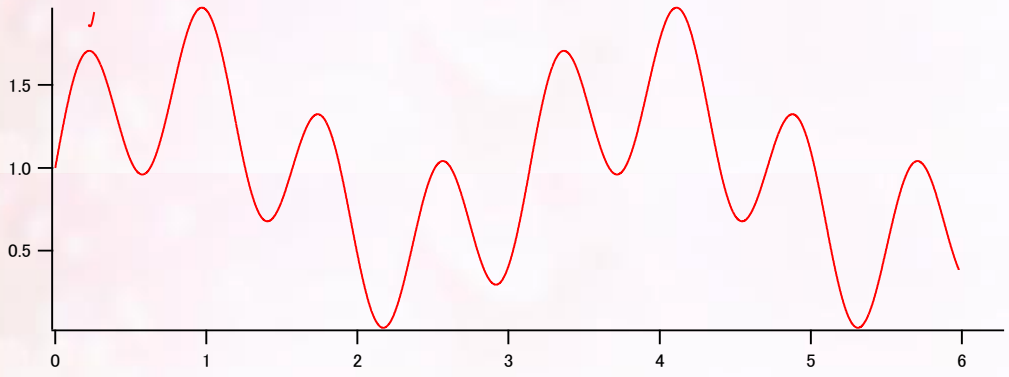


Results

Frequency filter



Original signal



7.6 Digital filter (as a digital signal processing)

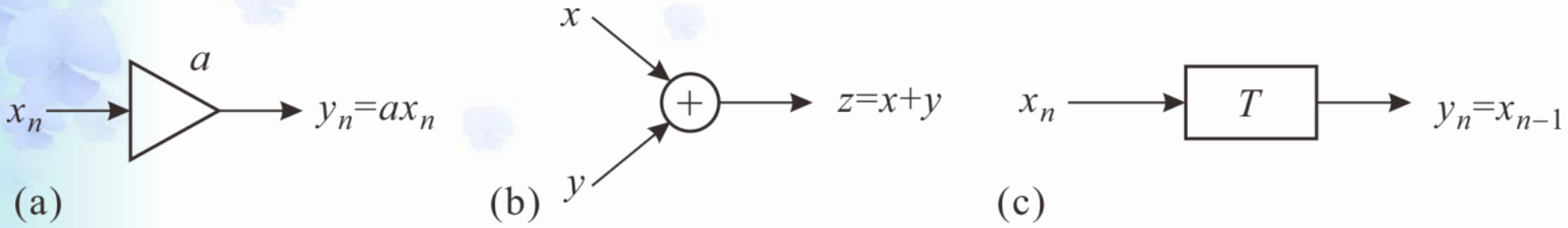
Digital filtering:

$$\{x_i\} = (x_0, x_1, \cdots)$$

$$\{y_i\} = (y_0, y_1, \cdots)$$

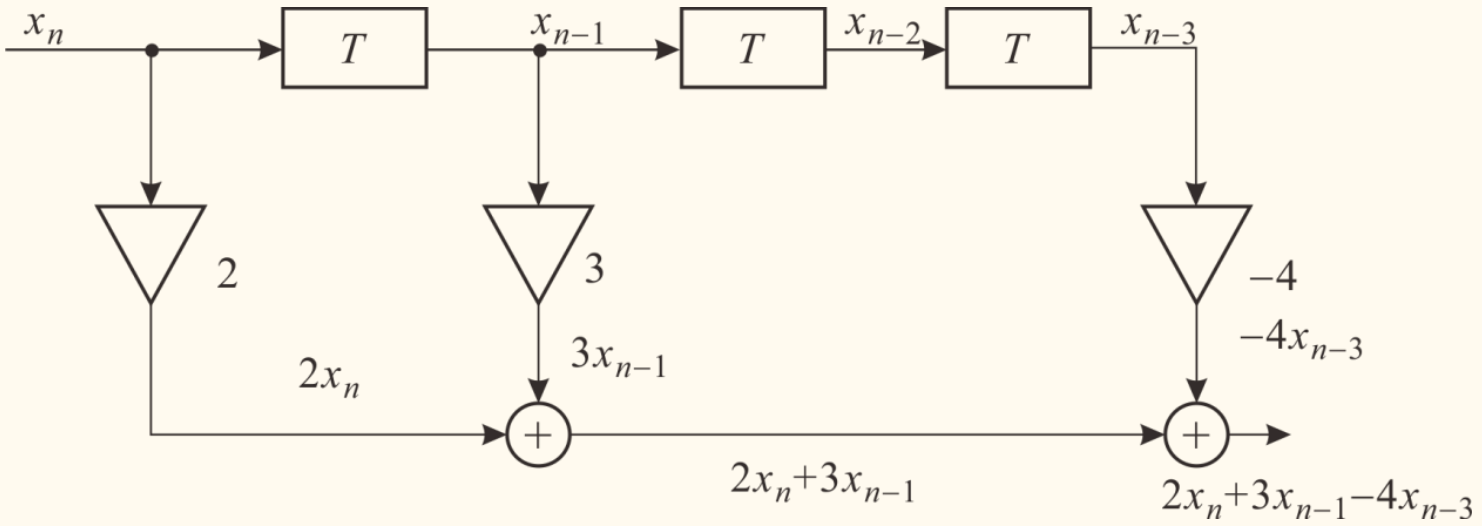
$$y_n = F(x_{n-k}, x_{n-k+1}, \cdots, x_n)$$

Block diagram representation of operations



constant multiplier adder delay (shift resistor)

Block diagram example



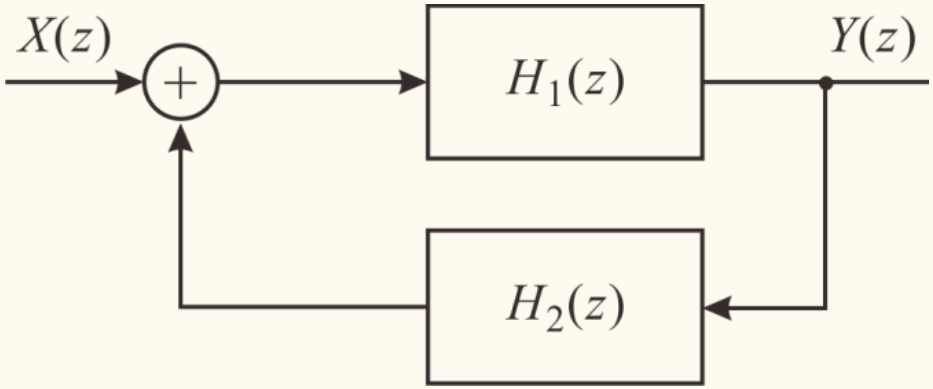
$$y_n = 2x_n + 3x_{n-1} - 4x_{n-3}$$

$$X(z) = \sum_{n=0}^{\infty} x_n z^{-n}, \quad Y(z) = \sum_{n=0}^{\infty} y_n z^{-n}$$

$$\begin{aligned} Y(z) &= 2X(z) + 3z^{-1}X(z) - 4z^{-3}X(z) \\ &= (2 + 3z^{-1} - 4z^{-3})X(z) \end{aligned}$$

$$\therefore H(z) \text{ (transfer function)} = 2 + 3z^{-1} - 4z^{-3}$$

Feedback and transfer function



$$Y(z) = H_1(z)W(z) = H_1(z)(X(z) + H_2(z)Y(z)),$$

$$\therefore Y(z) = \frac{H_1(z)}{1 - H_1(z)H_2(z)}X(z)$$

$$H(z) = \frac{H_1(z)}{1 - H_1(z)H_2(z)}$$

$$(\text{transfer function}) = \frac{(\text{direct gain})}{1 - (\text{feedback transfer gain})}$$