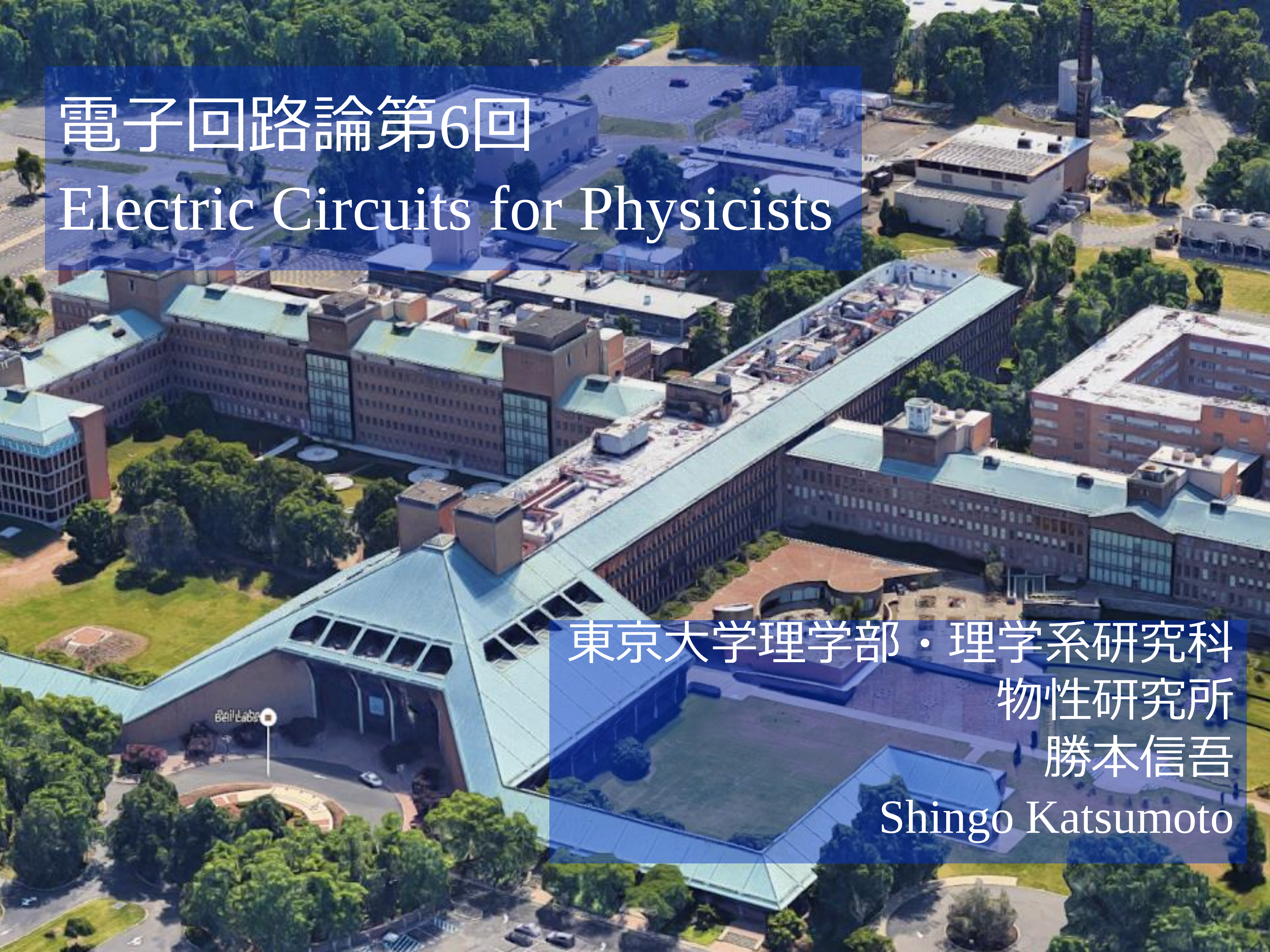


電子回路論第6回
Electric Circuits for Physicists

東京大学理学部・理学系研究科
物性研究所
勝本信吾
Shingo Katsumoto

Outline

4.3 Feedback control

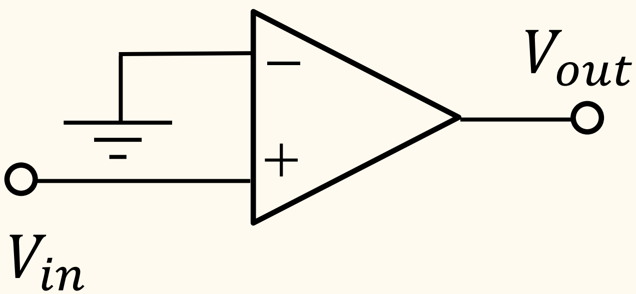
- 4.3.1 Disturbance and noise
- 4.3.2 PID control

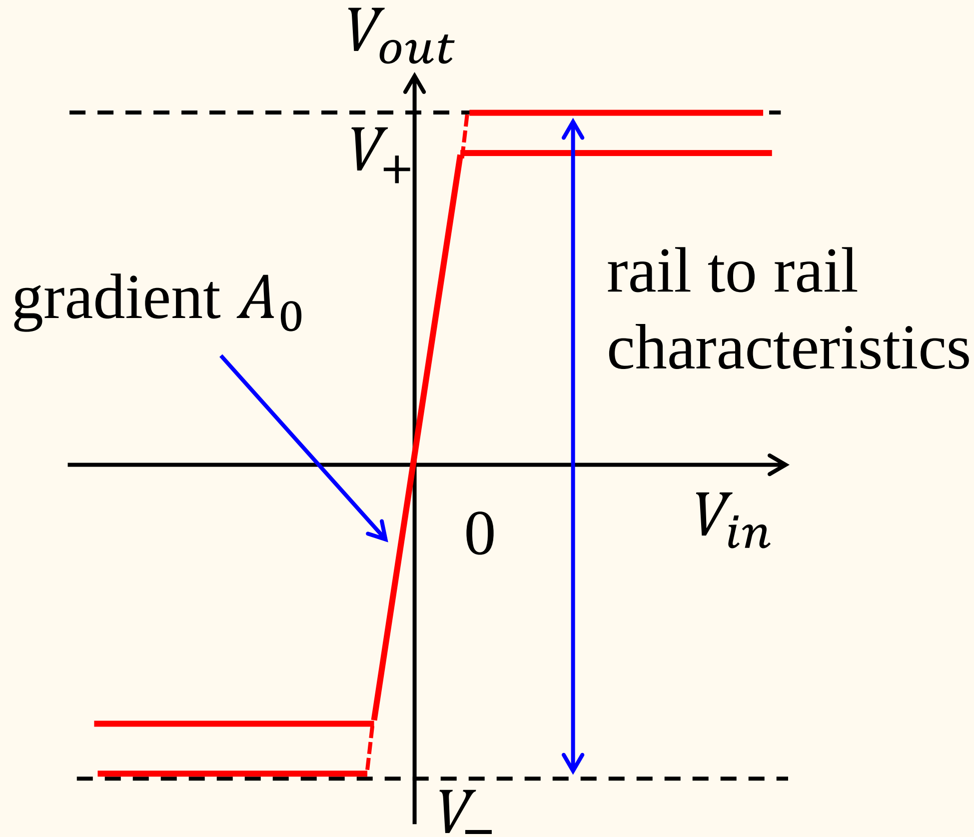
4.4 PN junction transistors

- 4.4.1 Diodes
- 4.4.2 Bipolar junction transistors

4.5 Field effect transistors

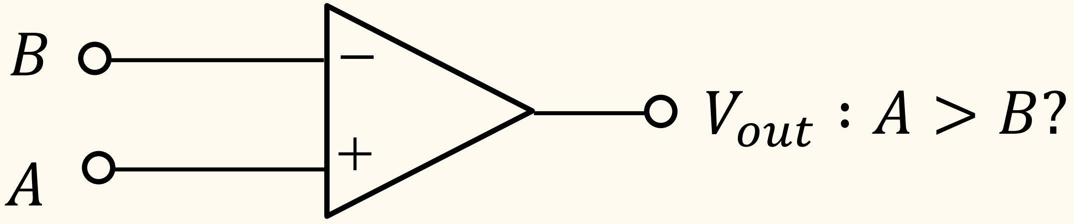
Comment: Use of OP-amp at saturation voltages





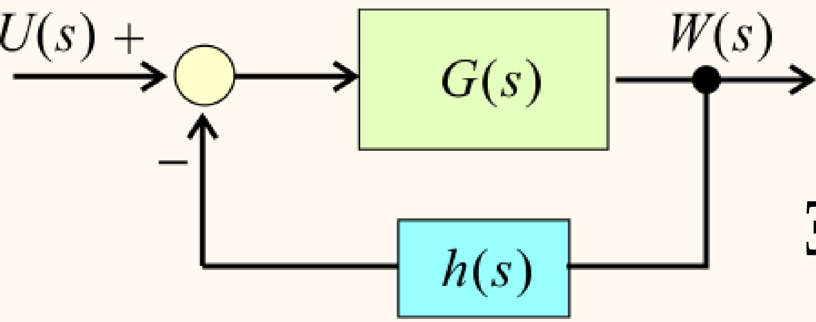
Compare V_{in} with 0

Comparator



Hurwitz criterion

Adolf Hurwitz
1859 - 1919



$$\Xi(s) = \frac{G(s)}{1 + h(s)G(s)}$$

Pole equation: $$(\text{denominator}) = a_n s^n + a_{n-1}s^{n-1} + \cdots + a_0$$
$$= a_n(s - p_1)\cdots(s - p_n) = 0$$

$$\forall j = 0, 1, \cdots, n: \quad a_j > 0 \text{ (or } < 0)$$ (Otherwise the system is unstable.)

Hurwitz matrix
$n \times n$

$$H = \begin{pmatrix} a_{n-1} & a_{n-3} & a_{n-5} & \cdots & 0 \\ a_n & a_{n-2} & a_{n-4} & \cdots & 0 \\ \hline 0 & a_{n-1} & a_{n-3} & \cdots & 0 \\ 0 & a_n & a_{n-2} & \cdots & 0 \\ \hline \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & a_0 \end{pmatrix}$$

Hurwitz criterion

Hurwitz determinants $H_j \equiv |H[1, \cdots, j; 1, \cdots, j]|$

$$H_1 = a_{n-1},\ H_2 = \begin{vmatrix} a_{n-1} & a_{n-3} \\ a_n & a_{n-2} \end{vmatrix},\ H_3 = \begin{vmatrix} a_{n-1} & a_{n-3} & a_{n-5} \\ a_n & a_{n-2} & a_{n-4} \\ 0 & a_{n-1} & a_{n-3} \end{vmatrix}, \cdots.$$

Hurwitz criterion

$$H_j > 0 \quad (j = 2, \cdots, n = 1)$$

$H_1, H_n > 0$ is trivial from the assumption.

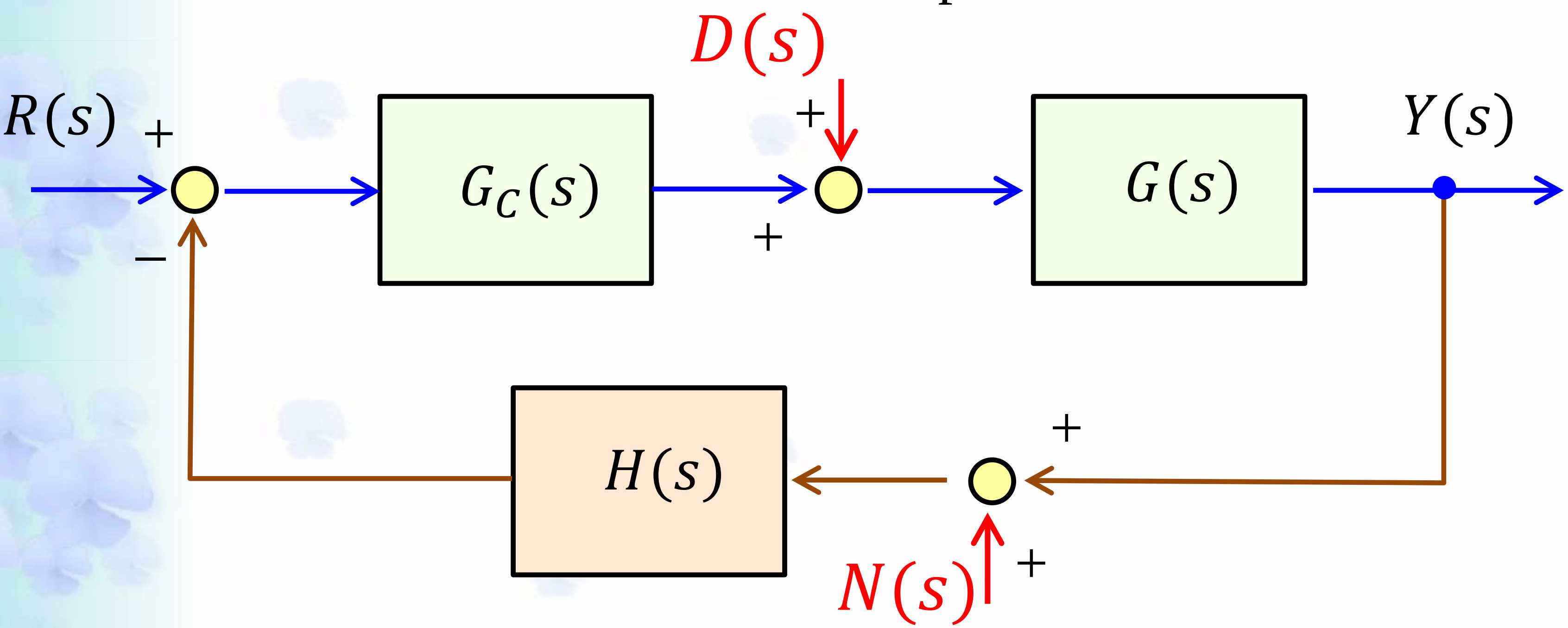
Another expression:

Divide the denominator to odd and even parts $O(s)$ and $E(s)$. If the zeros of $O(s)$ and $E(s)$ are aligned on the imaginary axis alternatively, the system is stable.

Disturbance and noise on feedback control

Circuit treatment of fluctuations:

- Prepare external power sources
- Express them as transfer functions



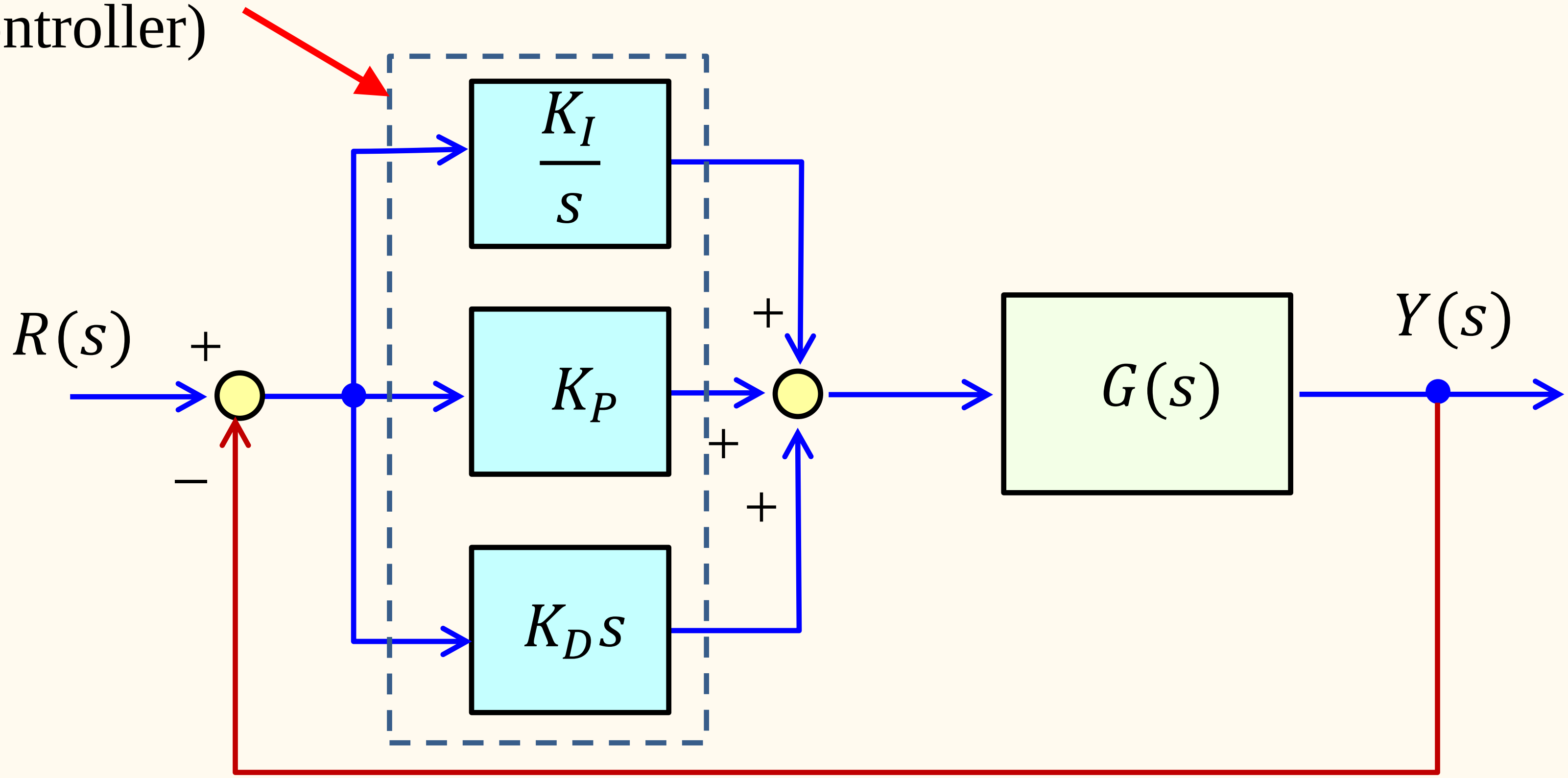
$$Y(s) = \frac{G(s)}{F(s)}[G_C(s)R(s) + D(s) + G_C(s)H(s)N(s)]$$

$$F(s) \equiv 1 + G_C(s)G(s)H(s)$$

PID control

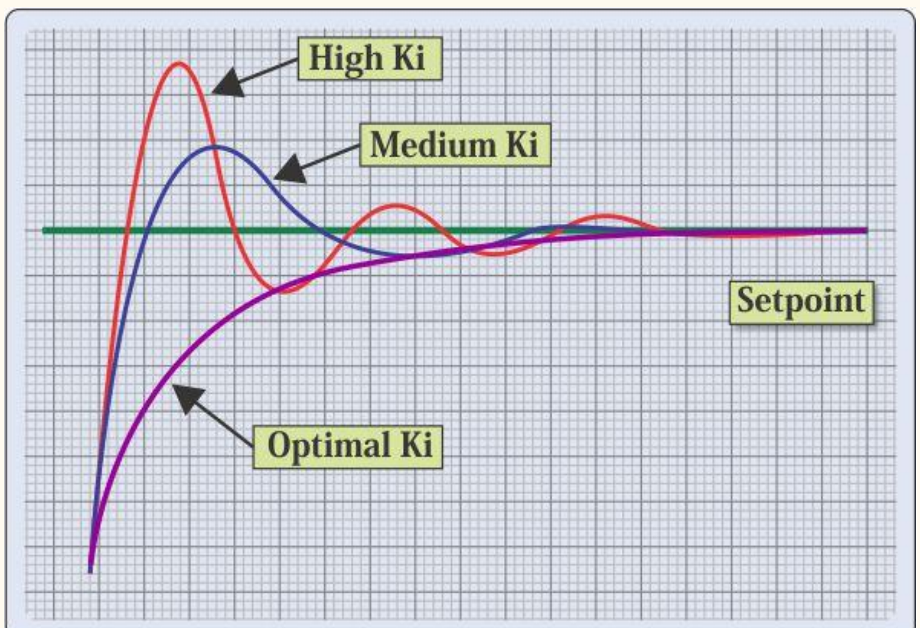
Compensator (controller)

P: proportional, I: integral, D: derivative



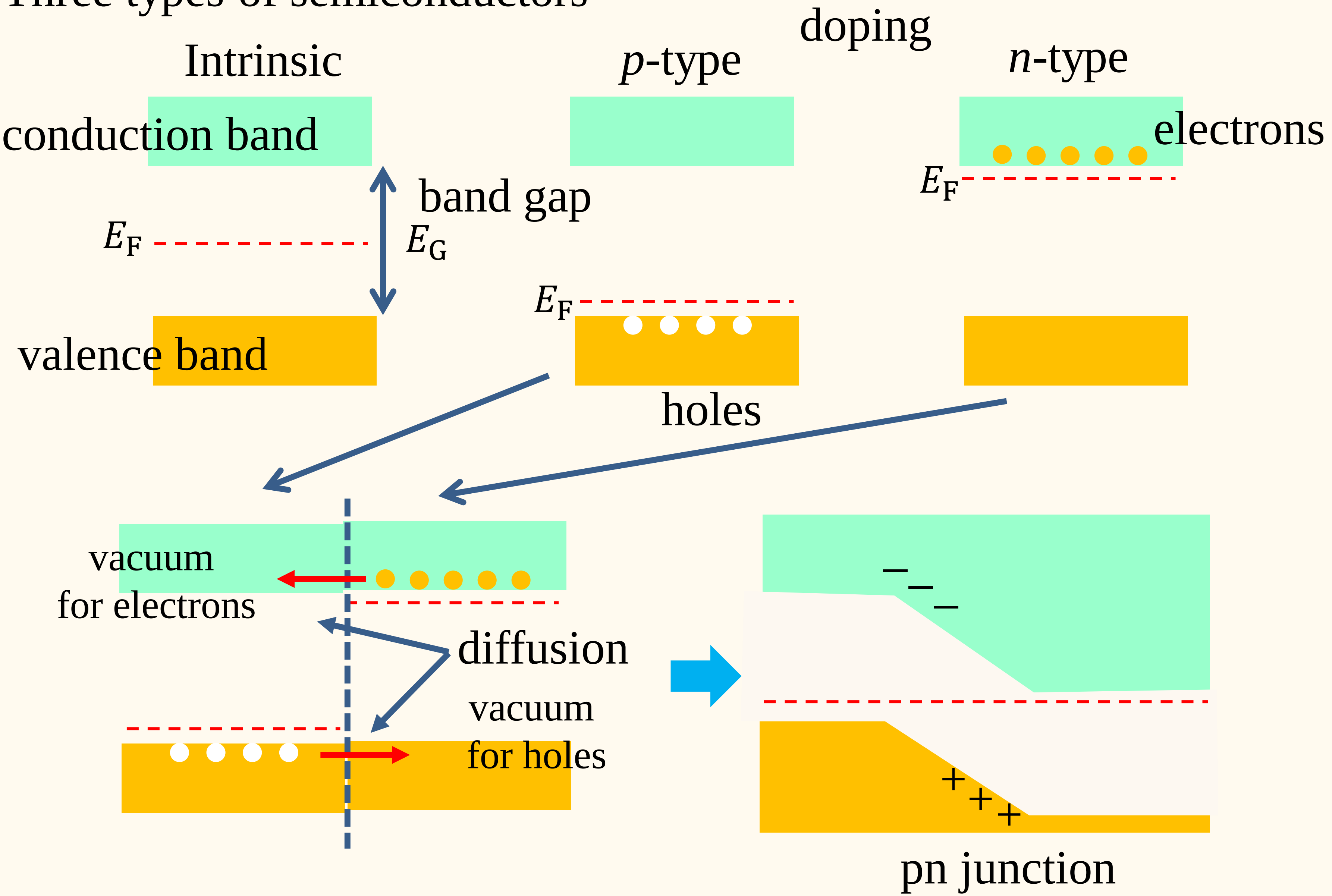
$$G_c(s) = K_P + \frac{K_I}{s} + K_D s$$

PID controllers



4.4 Example of active element: Transistors

Three types of semiconductors



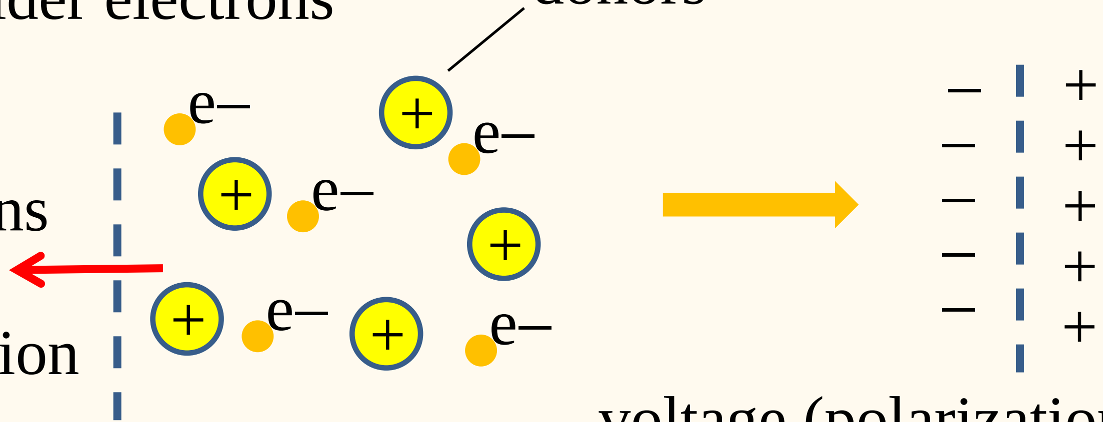
pn junction thermodynamics

Consider electrons

donors

Vacuum
for electrons

diffusion



voltage (polarization) → energy cost

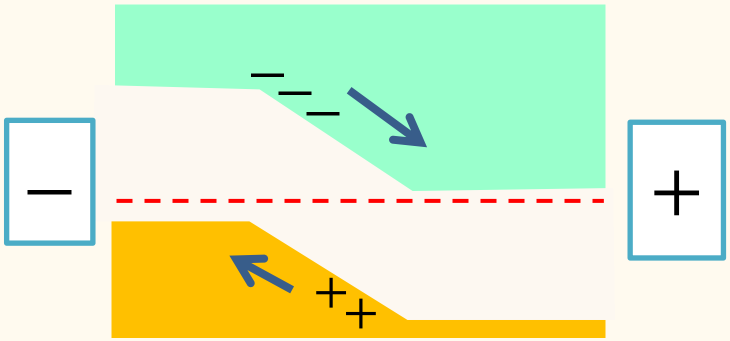
$$F = \underline{U} - T\underline{S}$$

Voltage (internal energy cost)

Diffusion (entropy)

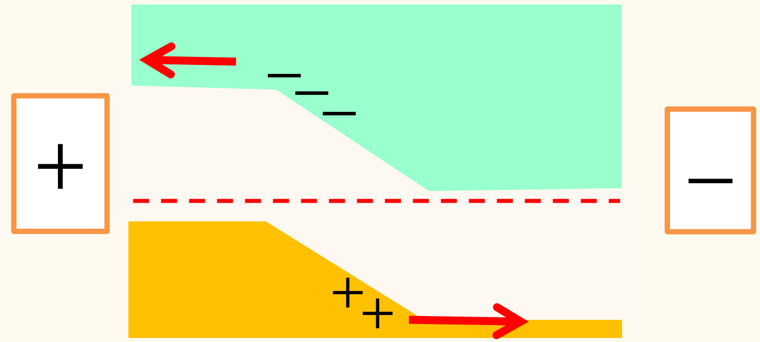
Minimization of F → Built-in (diffusion) voltage V_{bi}

4.4.1 I-V characteristics of pn junctions



Reverse bias

enhances V_{bi} : no go

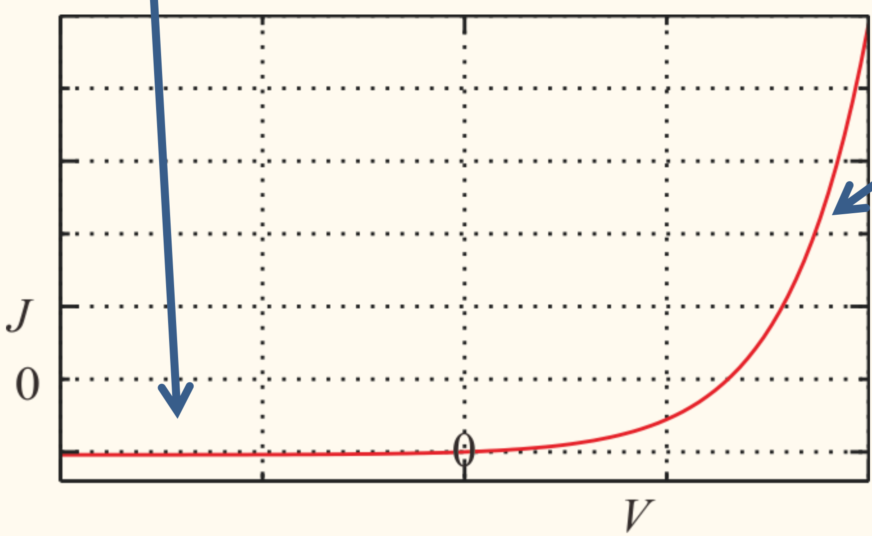


Forward bias

overcomes V_{bi} : go

Minority carrier injection

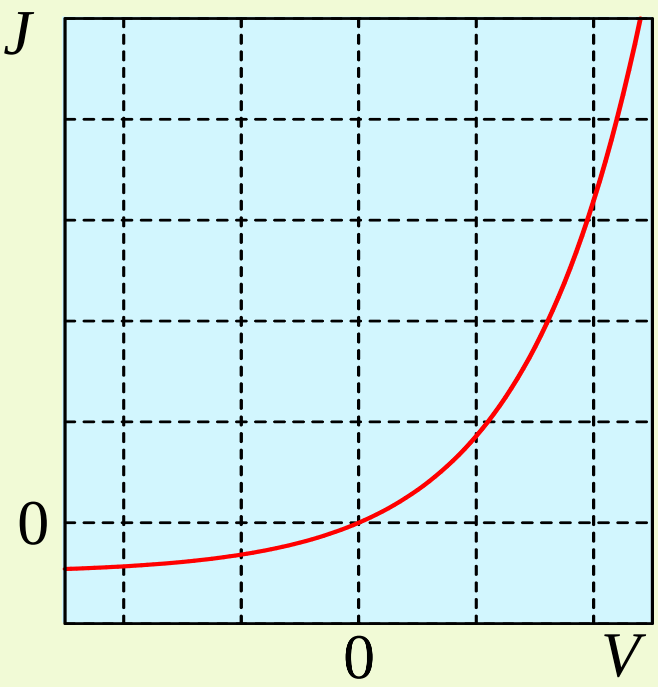
Rectification



$$J = J_0\left[\exp\left(\frac{eV}{k_{\mathrm{B}}T}\right) - 1\right]$$

Shockley theory

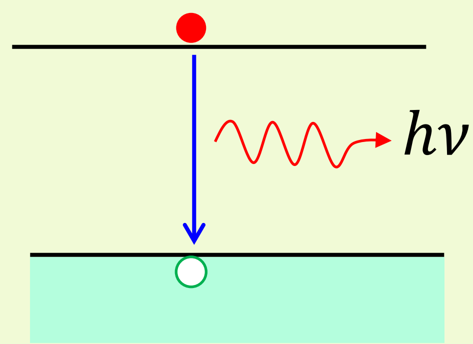
Injection of minority carriers



$$J = e(v_n n_p + v_p p_n) \left[\exp\frac{eV}{k_B T} - 1\right]$$

minority carrier current

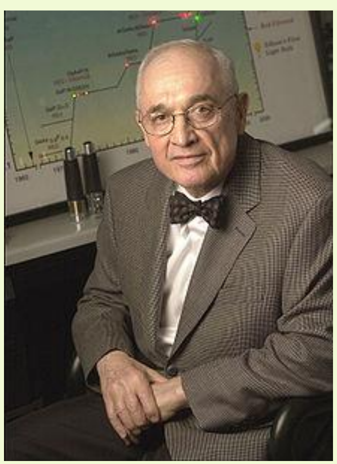
Barrier overflow



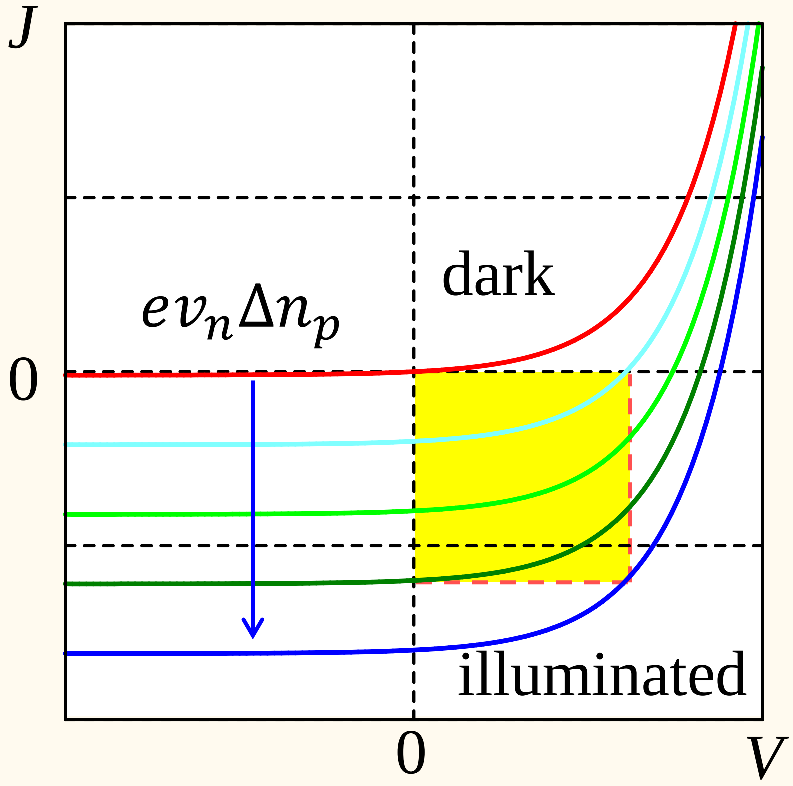
light emitting diode

Fate of injected minority carriers:
Radiative recombination

Nick Holonyak Jr.



Solar cell (injection of minority carriers with illumination)



$$J_{e0} = ev_n n_p \left[\exp\frac{eV}{k_B T} - 1\right]$$

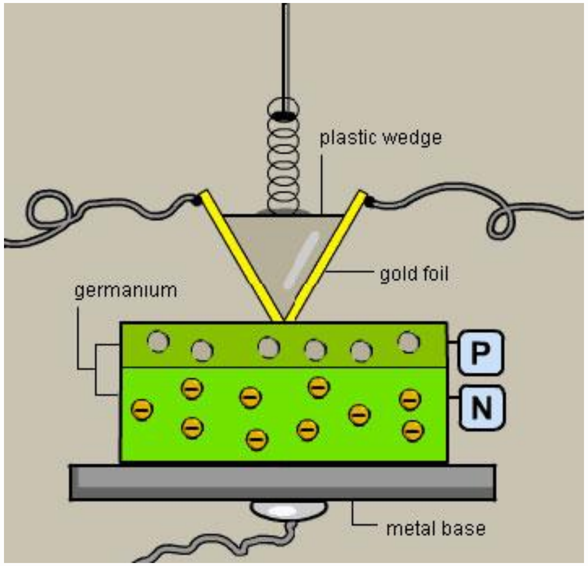
$$J_e = ev_n n_p \exp\frac{eV}{k_B T} - ev_n(n_p + \Delta n_p)$$

$$= J_{n0} - \underline{ev_n \Delta n_p}$$

External injection

Gerald Pearson,
Daryl Chapin
and Calvin Fuller
at Bell labs. 1954

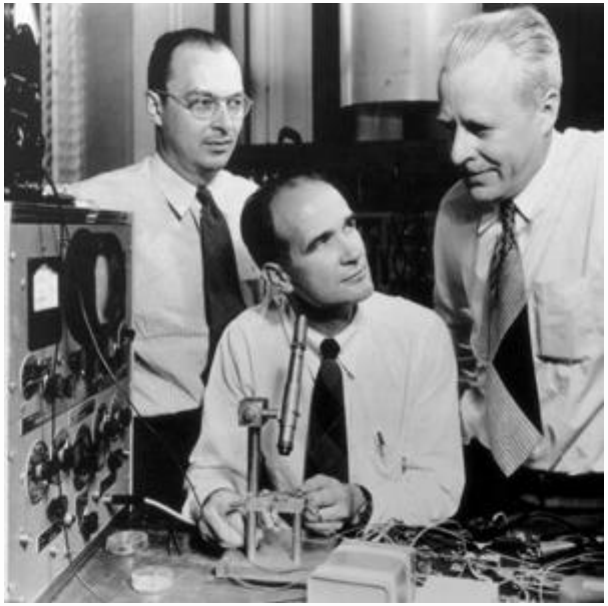
4.3.2 Discovery and invention of bi-polar transistors



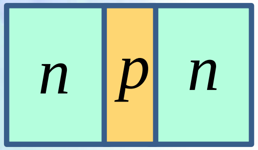
The first point contact transistor

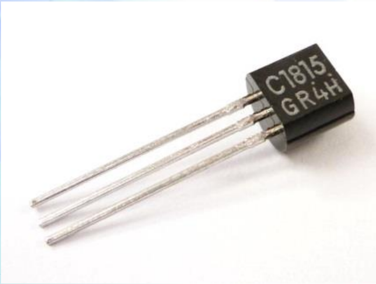
(Dec. 1947
The paper published in June 1948.)

John Bardeen, William Shockley, Walter Brattain 1948 Bell Labs.

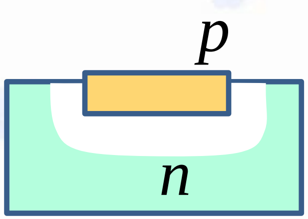


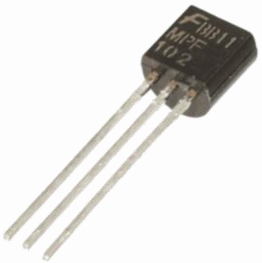
Bipolar junction transistor



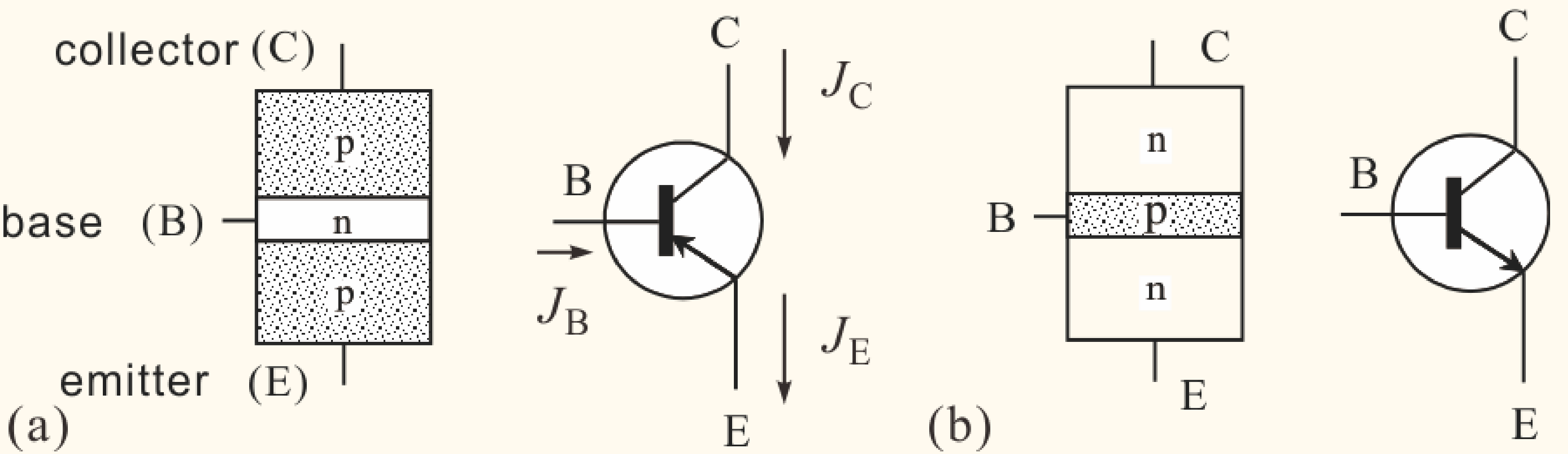


Field effect transistor





Bipolar transistor structures and symbols



PNP type

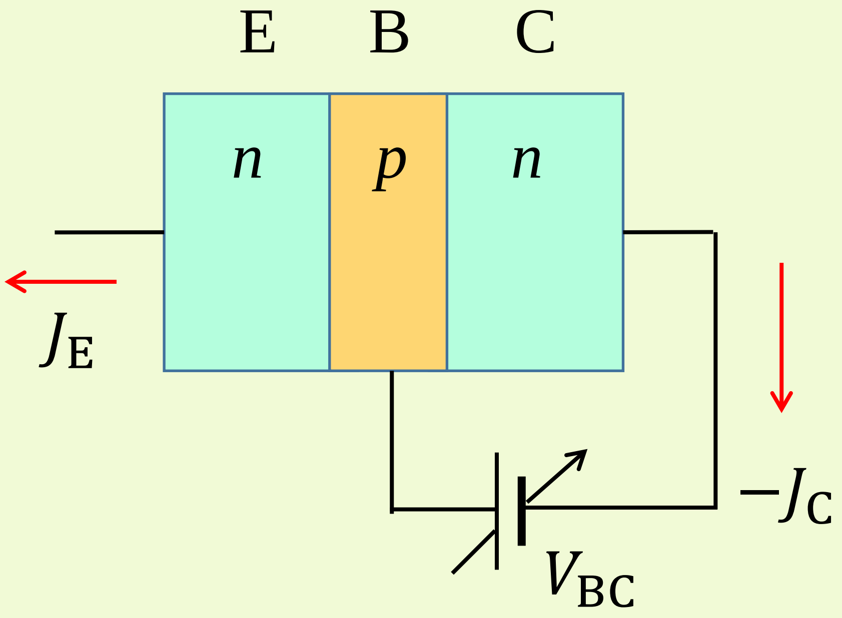
$$L_B < L_h$$

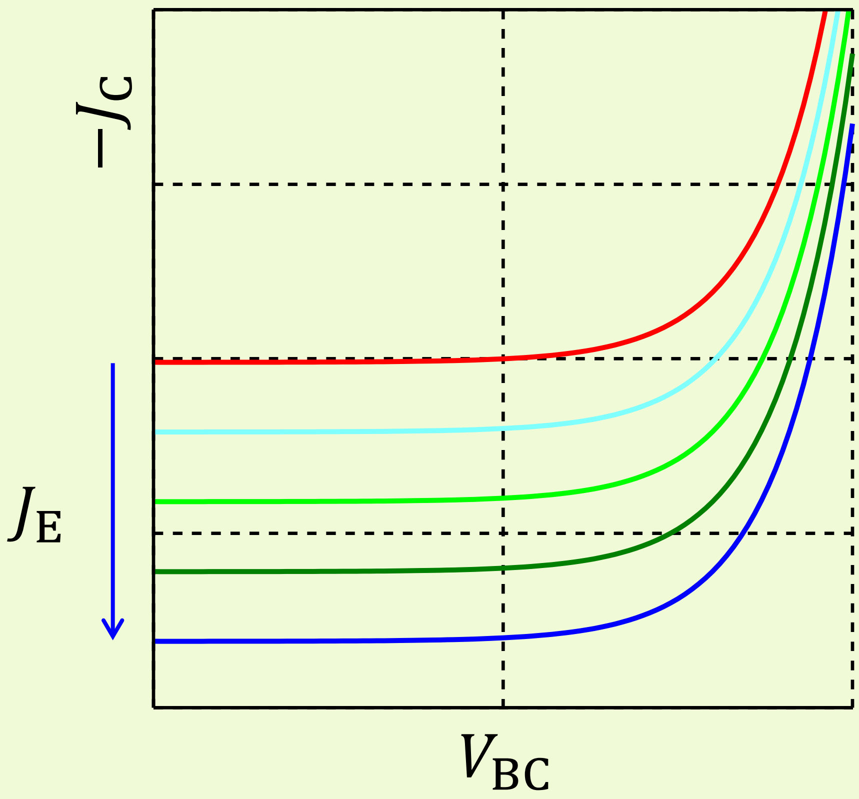
NPN type

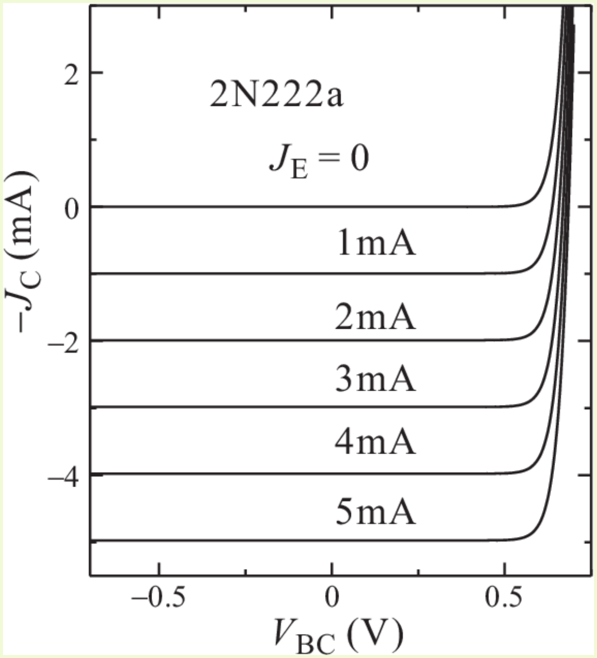
$$L_B < L_e$$

Similar characteristics PNP and NPN: complementary

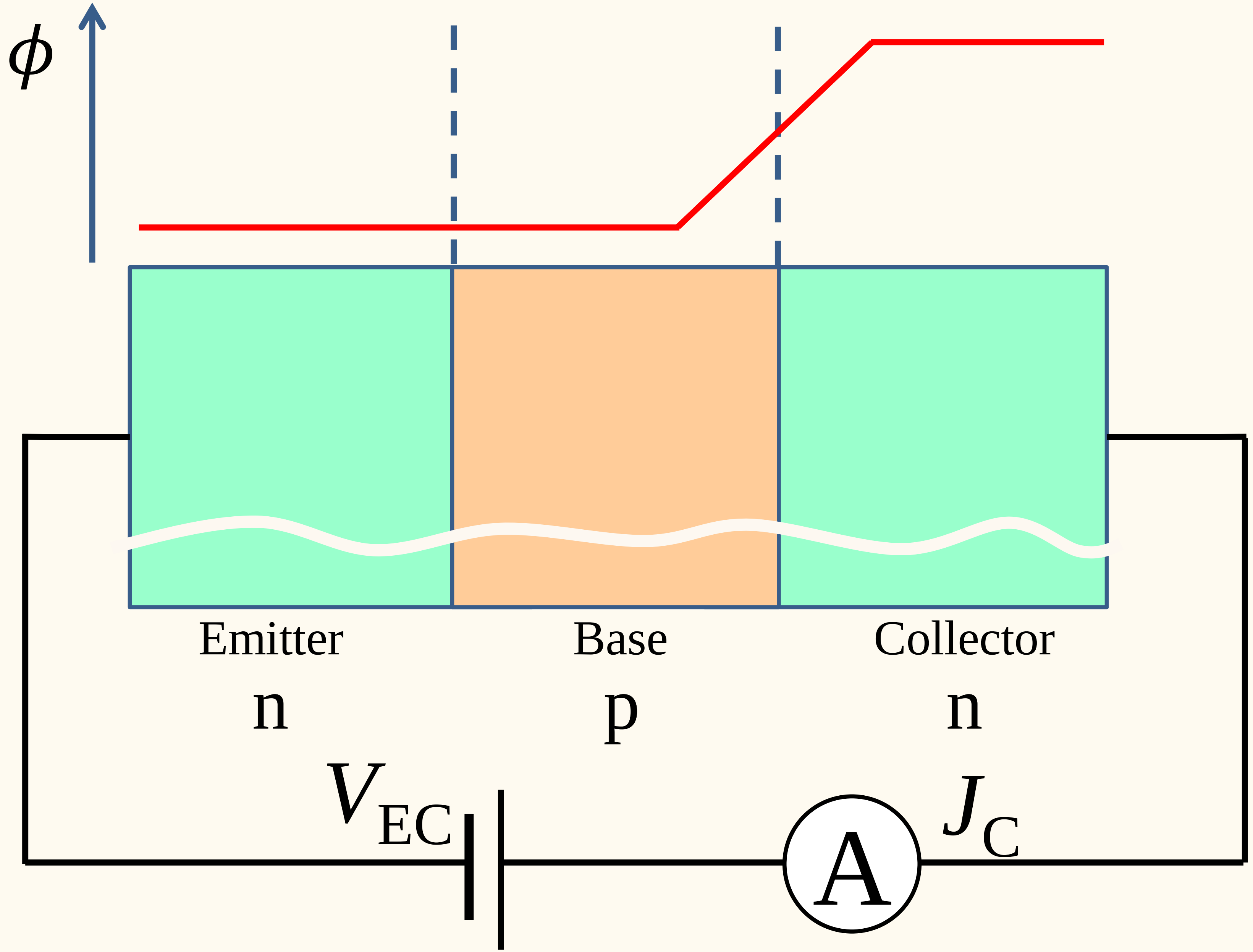
Base-Collector characteristics



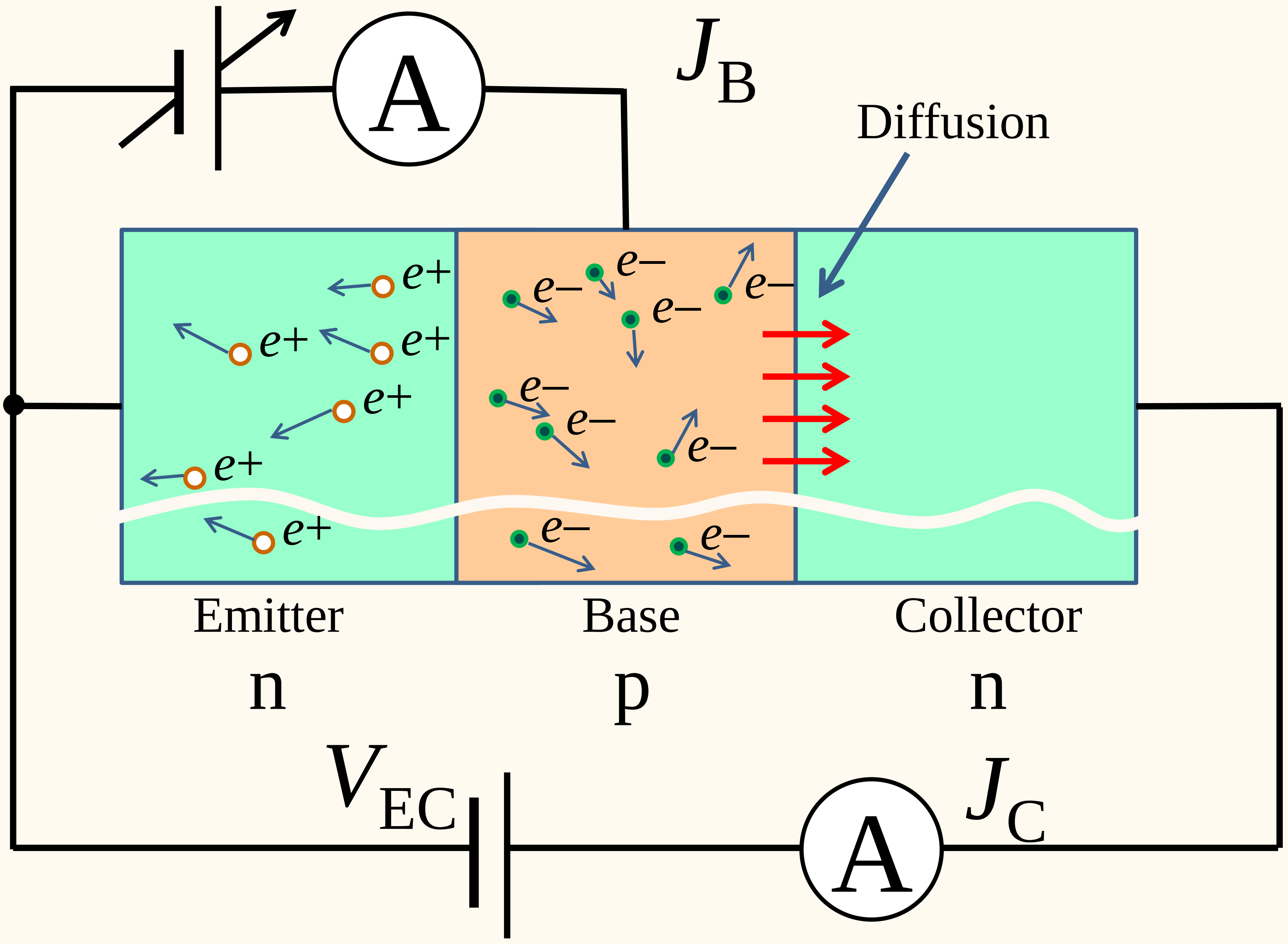




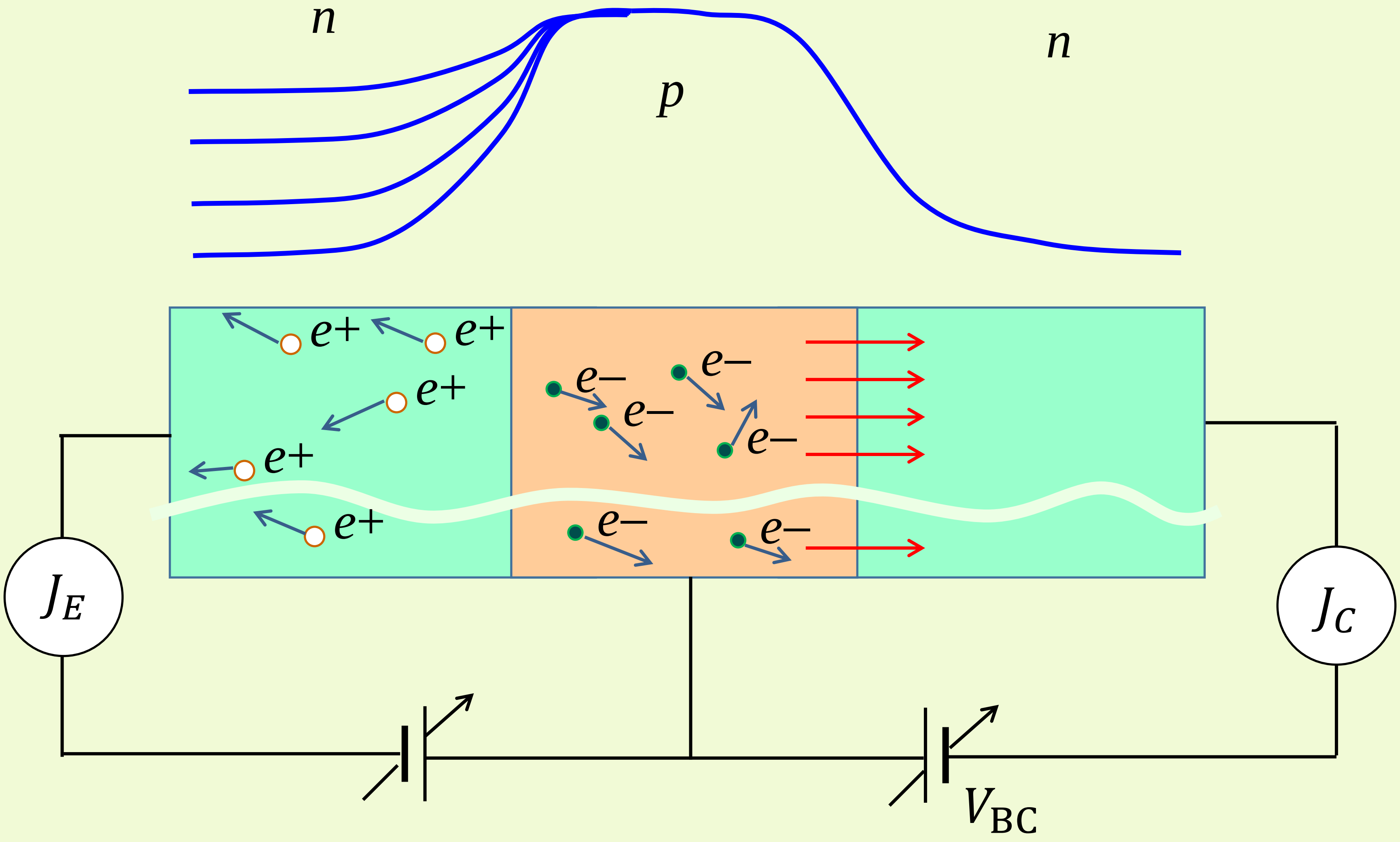
How a bipolar transistor amplifies?



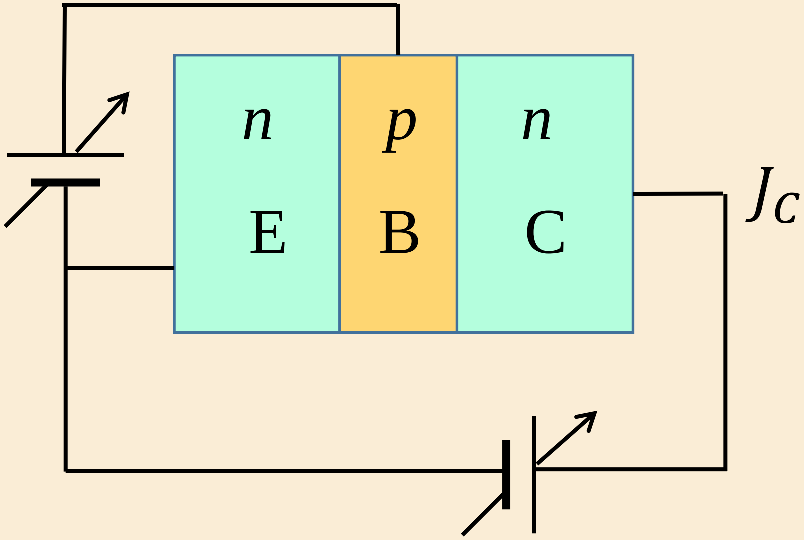
How a bipolar transistor amplifies?

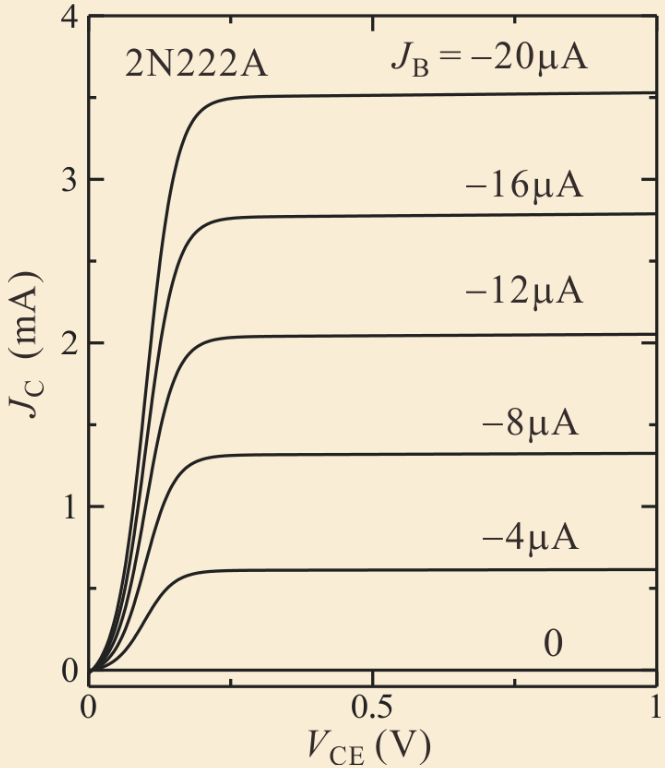


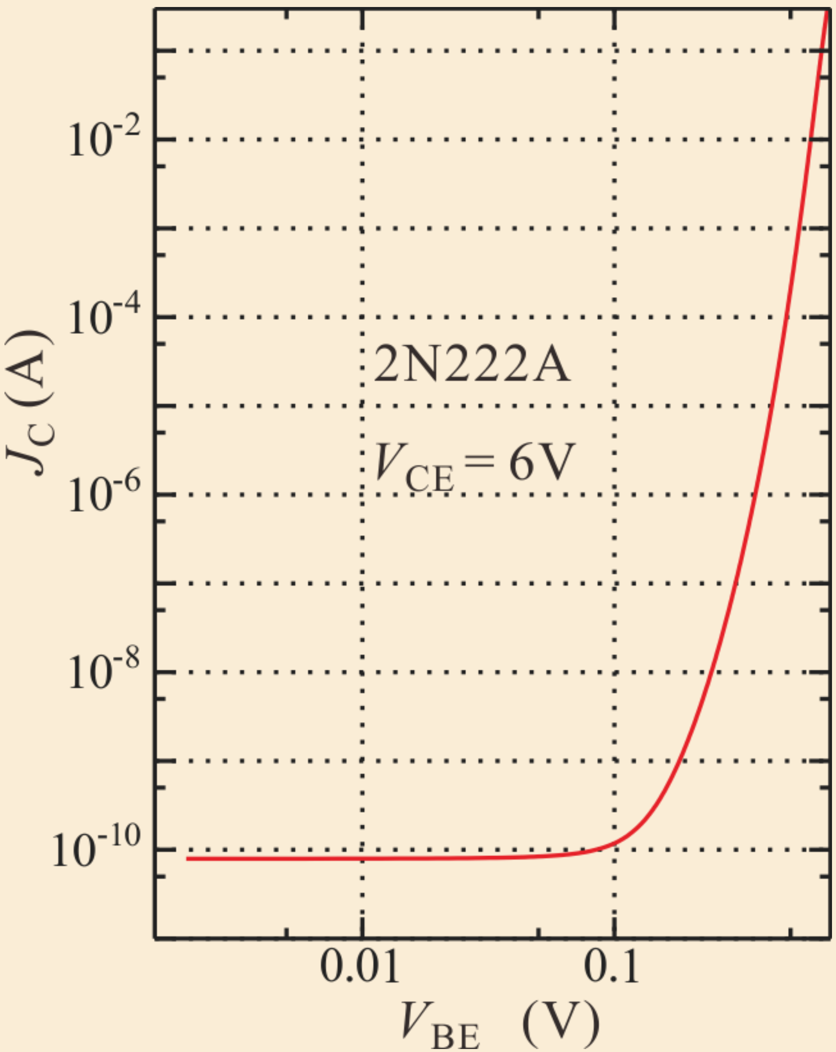
Base-Collector characteristics



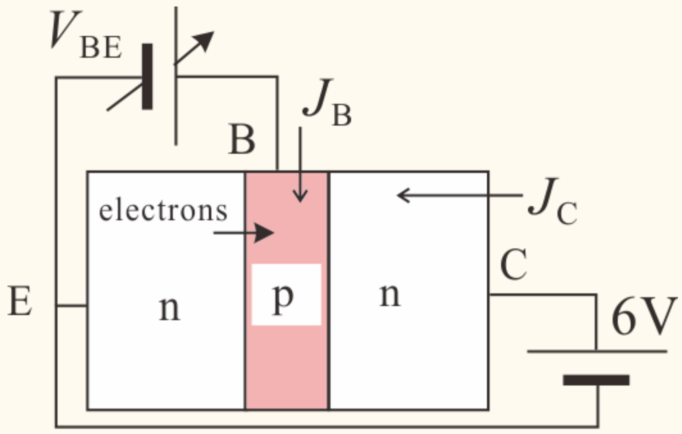
Collector-Emitter characteristics





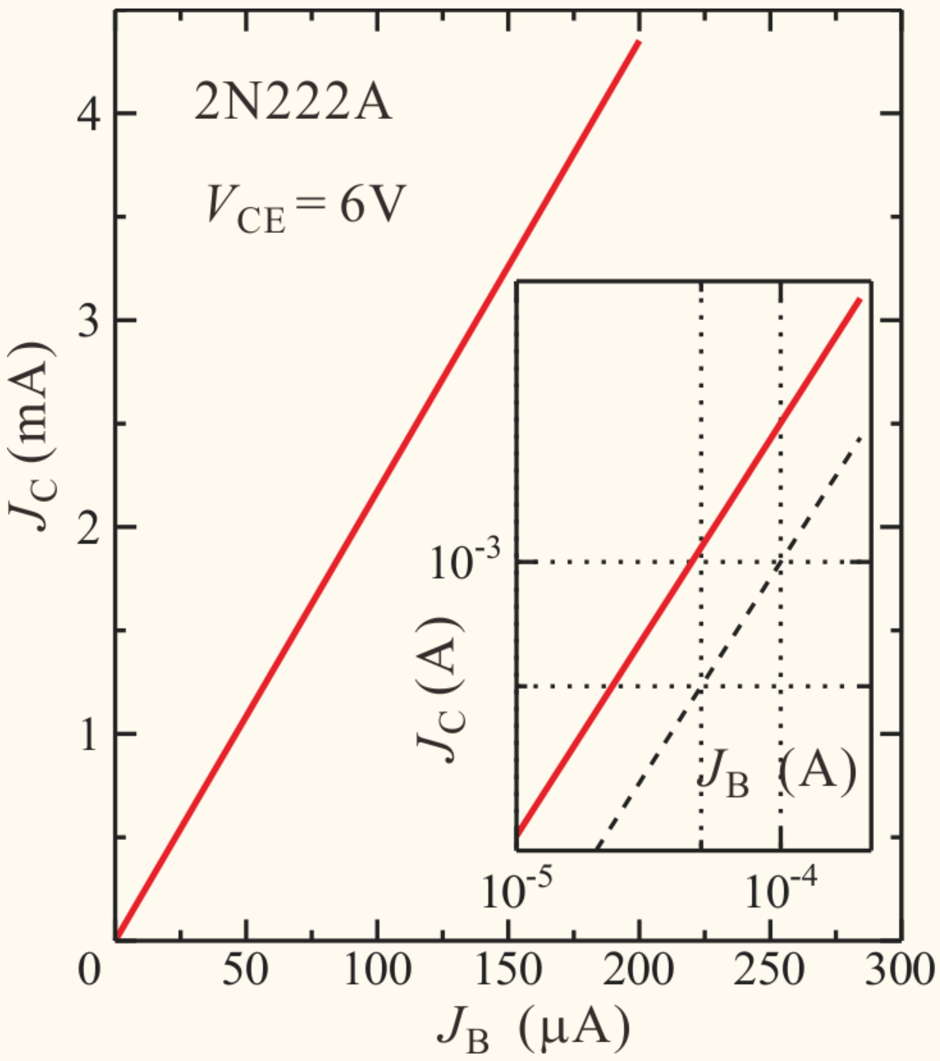


Current amplification : Linearize with quantity selection

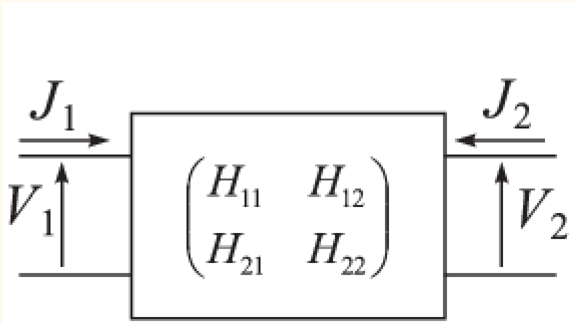


$$J_C = \underline{h_{FE}}\, J_B$$

Emitter-common current gain

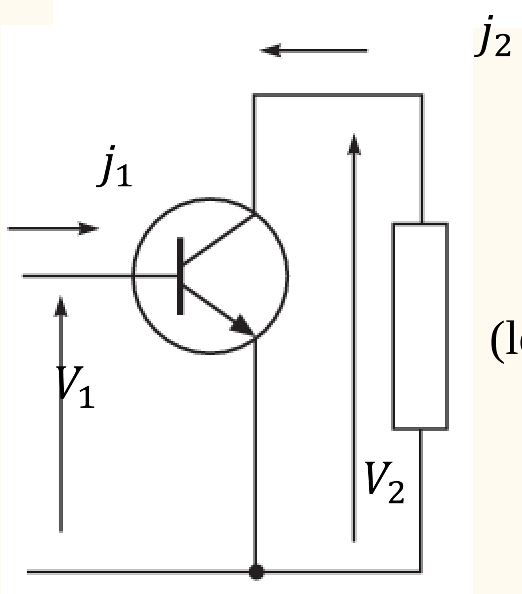


Linear approximation of bipolar transistor



Hybrid matrix

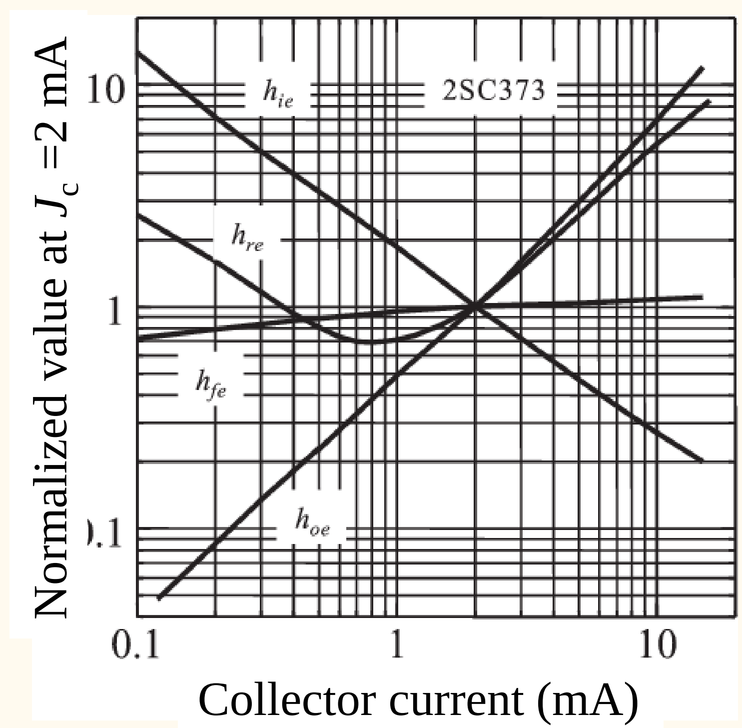
$$\begin{pmatrix} V_1 \\ J_2 \end{pmatrix} = \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} \begin{pmatrix} J_1 \\ V_2 \end{pmatrix} .$$



$$\begin{pmatrix} v_1 \\ j_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} j_1 \\ v_2 \end{pmatrix} = \begin{pmatrix} h_i & h_r \\ h_f & h_o \end{pmatrix} \begin{pmatrix} j_1 \\ v_2 \end{pmatrix}$$

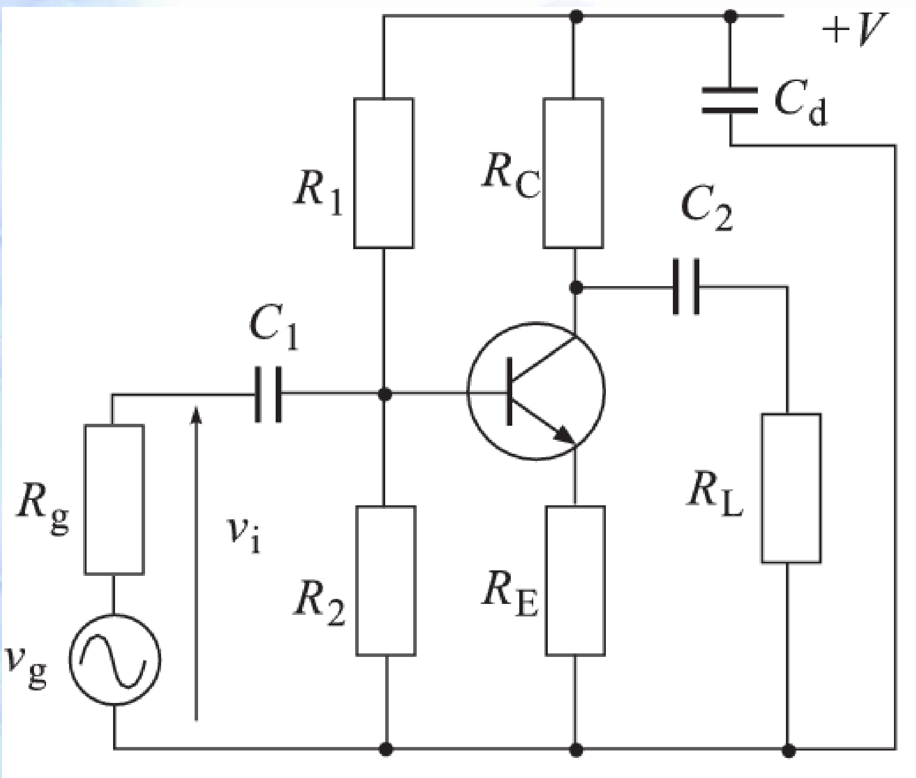
h-parameters

(lower case:
local linear approximation)



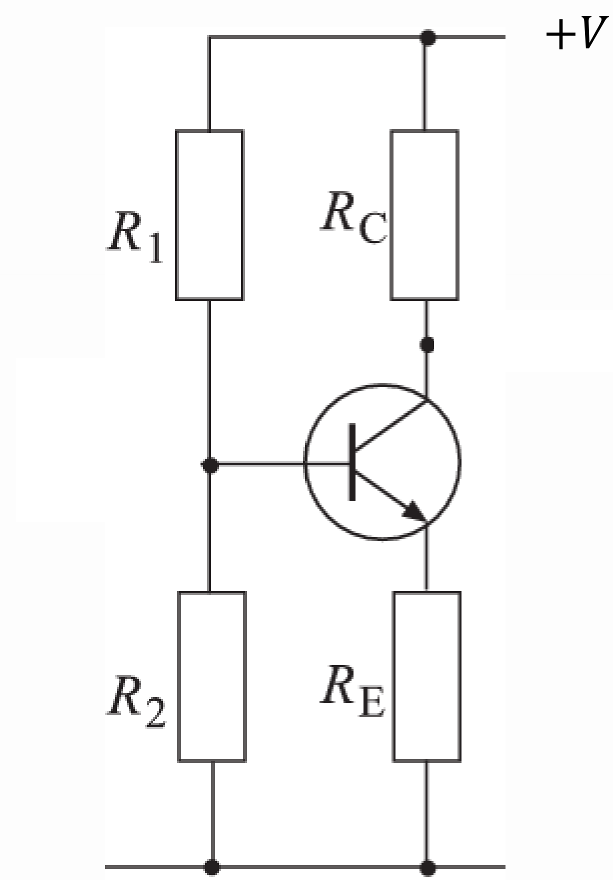
Concept of bias circuits for non-linear devices

Common emitter amplifier



For bias (dc) circuits

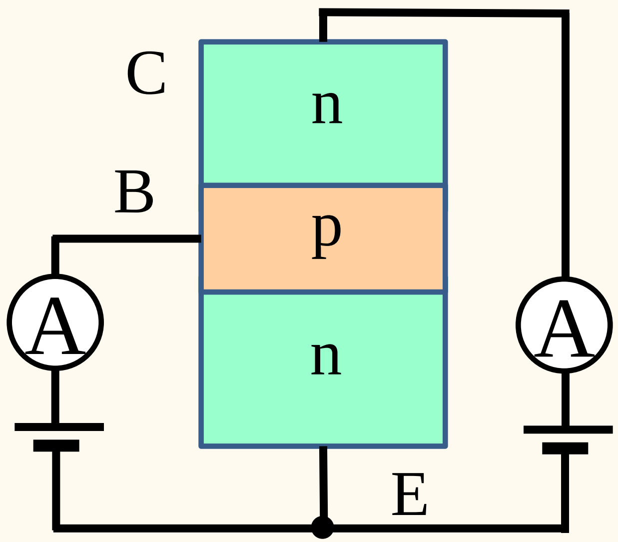
All the capacitors can be viewed as break line.

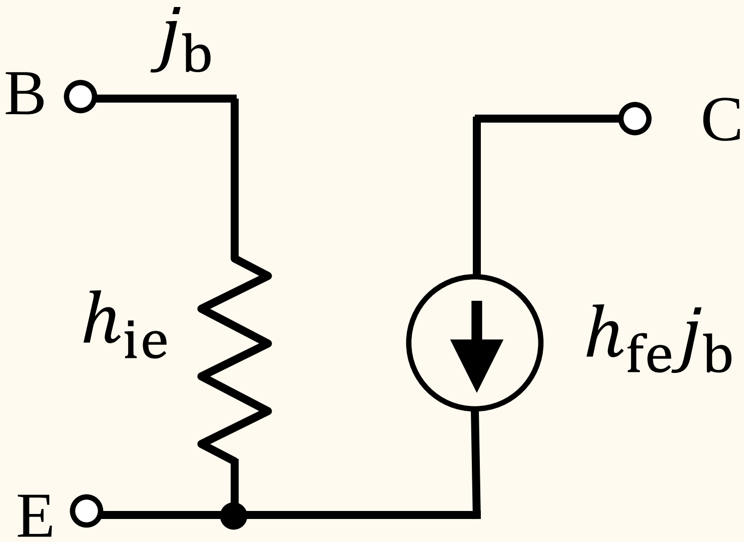


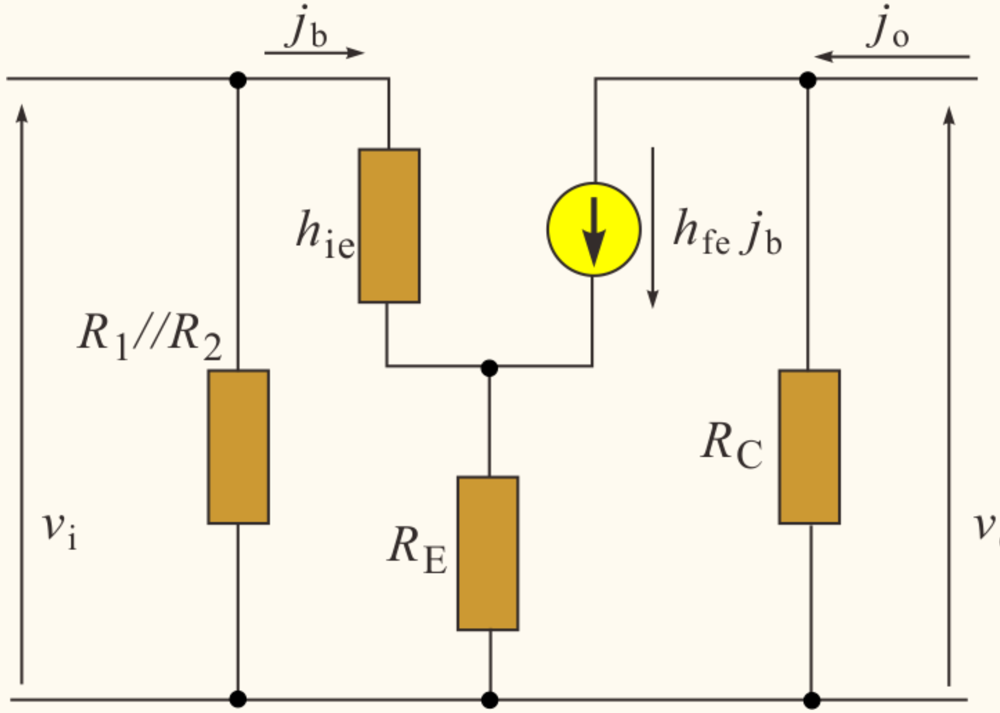
For small amplitude (high-frequency) circuits

All the capacitors can be viewed as short circuits.

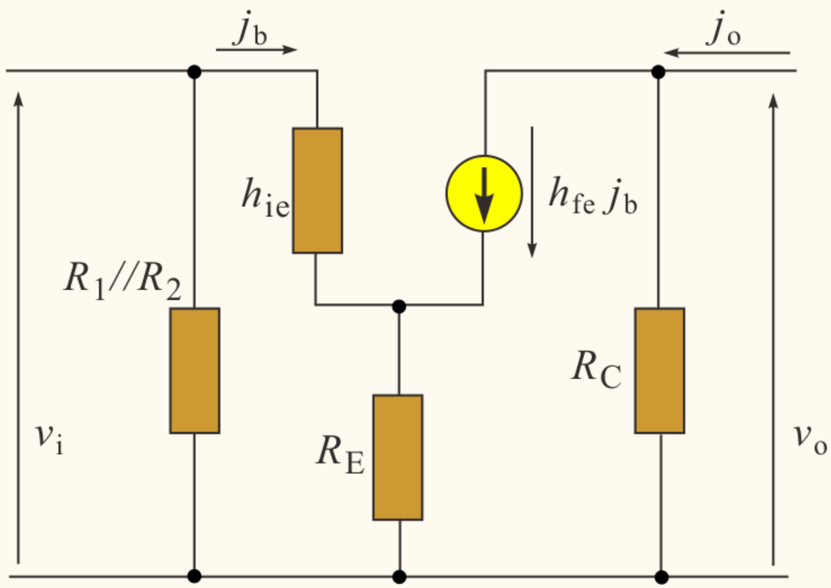
Concept of equivalent circuit

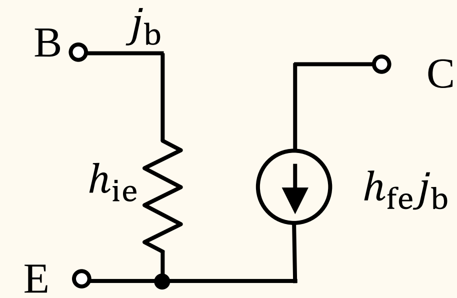


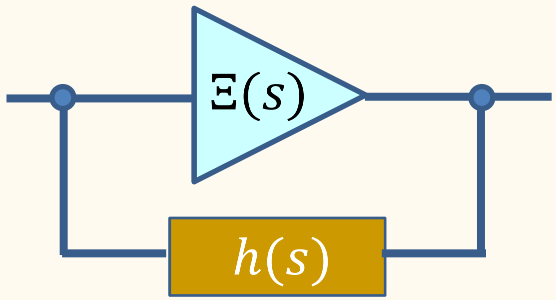


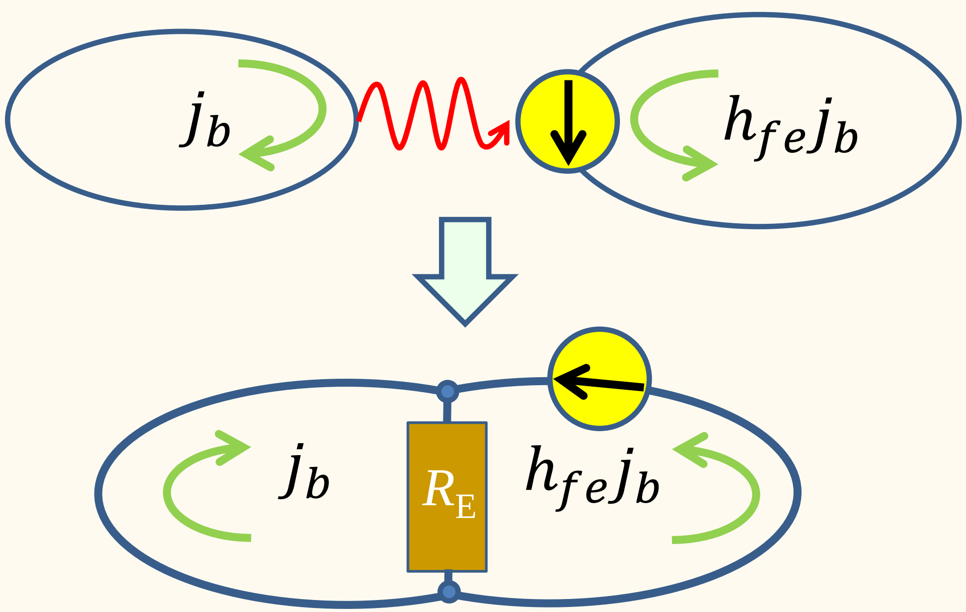


Concept of equivalent circuit: Where is feedback?







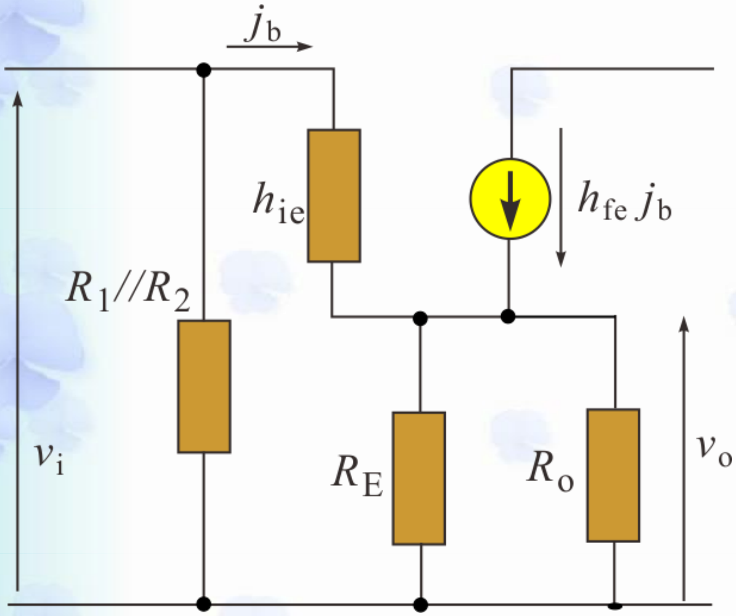


$$A = \frac{v_o}{v_i}$$

$$= \frac{h_{fe}R_C}{h_{ie} + R_E(1 + h_{fe})}$$

$$\approx \frac{R_C}{R_E} \quad h_{fe} \gg 1$$

Current amplification: Emitter follower

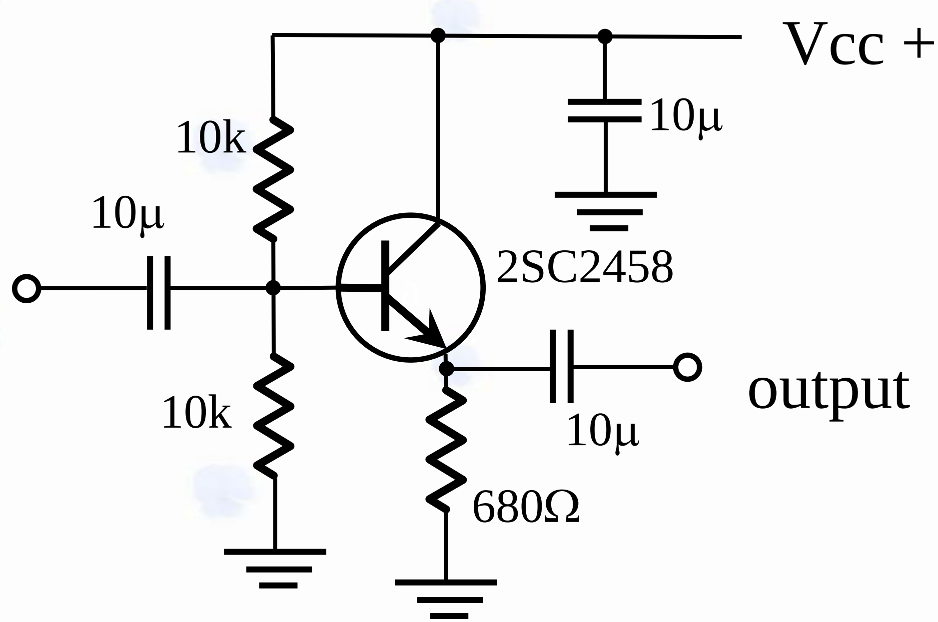


$$\frac{v_o}{v_i} = \frac{j_b(1 + h_{fe})(R_E \parallel R_o)}{j_b[h_{ie} + (1 + h_{fe})(R_E \parallel R_o)]}$$

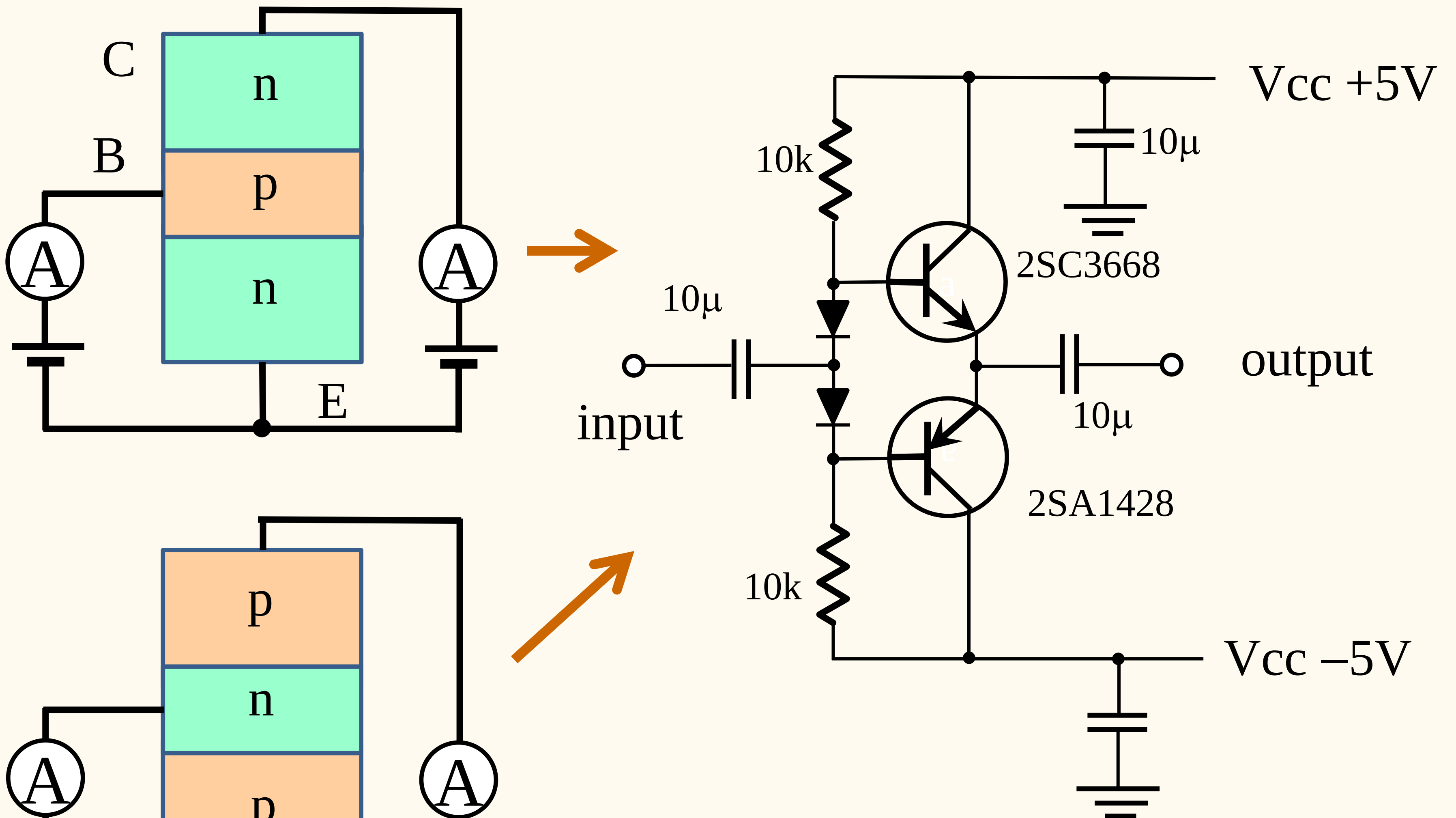
$$\approx 1 \qquad (h_{fe} \gg 1)$$

v_o does not depend on load resistance

⇒ Very low output resistance



Complementary transistors

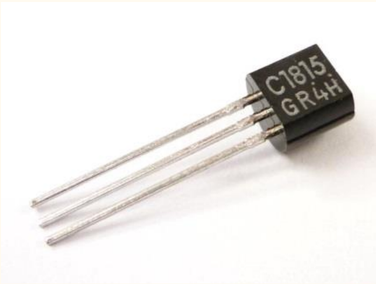


Symmetric characteristics: Complementary

Symmetric: Small collector current (idling current) for zero input.

Example of transistor datasheet

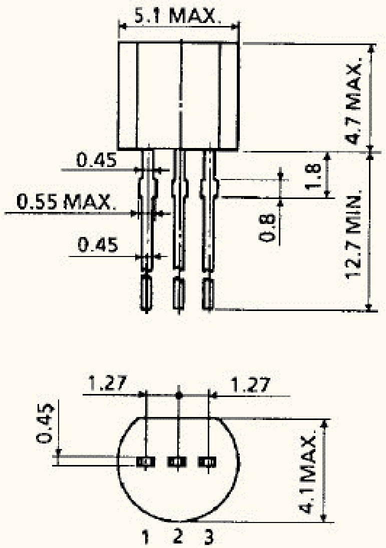
TOSHIBA 2SC1815(L)



TOSHIBA Transistor Silicon NPN Epitaxial Type (PCT process)

2SC1815(L)

Unit: mm



1. EMITTER
2. COLLECTOR
3. BASE

JEDEC	TO-92
JEITA	SC-43
TOSHIBA	2-5F1B

Audio Frequency Voltage Amplifier Applications

Low Noise Amplifier Applications

- High breakdown voltage, high current capability
  : $V_{CEO} = 50$ V (min), $I_C = 150$ mA (max)
- Excellent linearity of h_{FE}
  : h_{FE} (2) = 100 (typ.) at $V_{CE} = 6$ V, $I_C = 150$ mA
  : h_{FE} ($I_C = 0.1$ mA)/h_{FE} ($I_C = 2$ mA) = 0.95 (typ.)
- Low noise: NF = 0.2dB (typ.) (f = 1 kHz).
- Complementary to 2SA1015 (L). (O, Y, GR class).

Example of transistor datasheet

TOSHIBA Transistor Silicon NPN Epitaxial Type (PCT process)

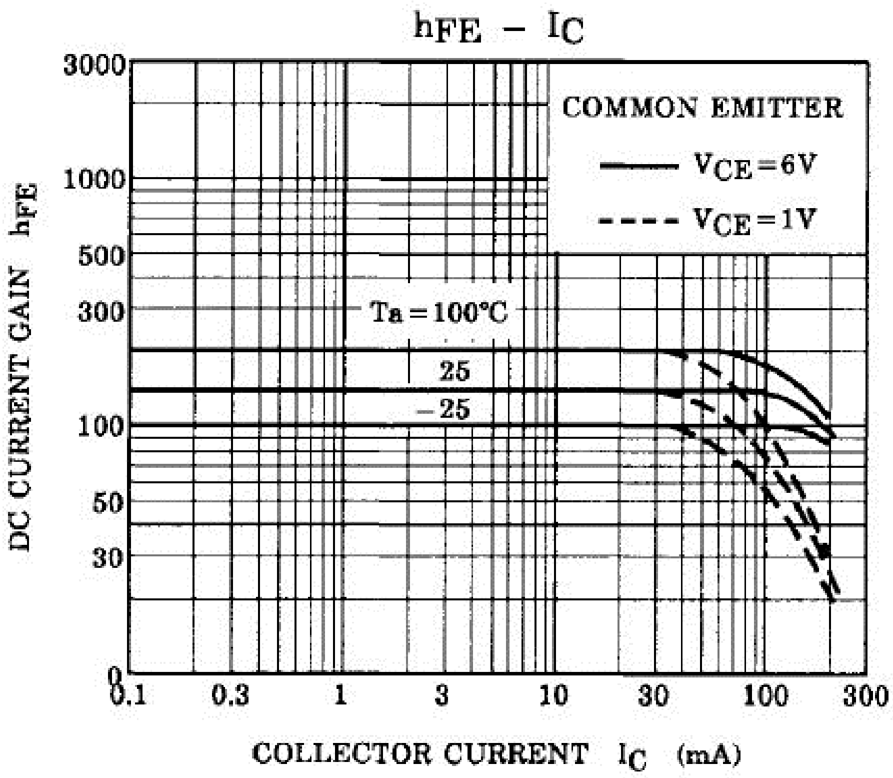
2SC1815(L)

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 60 V, I_E = 0	—	—	0.1	μA
Emitter cut-off current		I_{EBO}	V_{EB} = 5 V, I_C = 0	—	—	0.1	μA
DC current gain		$h_{FE\ (1)}$ (Note)	V_{CE} = 6 V, I_C = 2 mA	70	—	700	
		$h_{FE\ (2)}$	V_{CE} = 6 V, I_C = 150 mA	25	100	—	
Saturation voltage	Collector-emitter	$V_{CE\ (sat)}$	I_C = 100 mA, I_B = 10 mA	—	0.1	0.25	V
	Base-emitter	$V_{BE\ (sat)}$	I_C = 100 mA, I_B = 10 mA	—	—	1.0	
Transition frequency		f_T	V_{CE} = 10 V, I_C = 1 mA	80	—	—	MHz
Collector output capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1 MHz	—	2.0	3.5	pF
Base intrinsic resistance		$r_{bb'}$	V_{CE} = 10 V, I_E = −1 mA, f = 30 MHz	—	50	—	Ω
Noise figure		NF (1)	V_{CE} = 6 V, I_C = 0.1 mA R_G = 10 kΩ, f = 100 Hz	—	0.5	6	dB
		NF (2)	V_{CE} = 6 V, I_C = 0.1 mA R_G = 10 kΩ, f = 1 kHz	—	0.2	3	

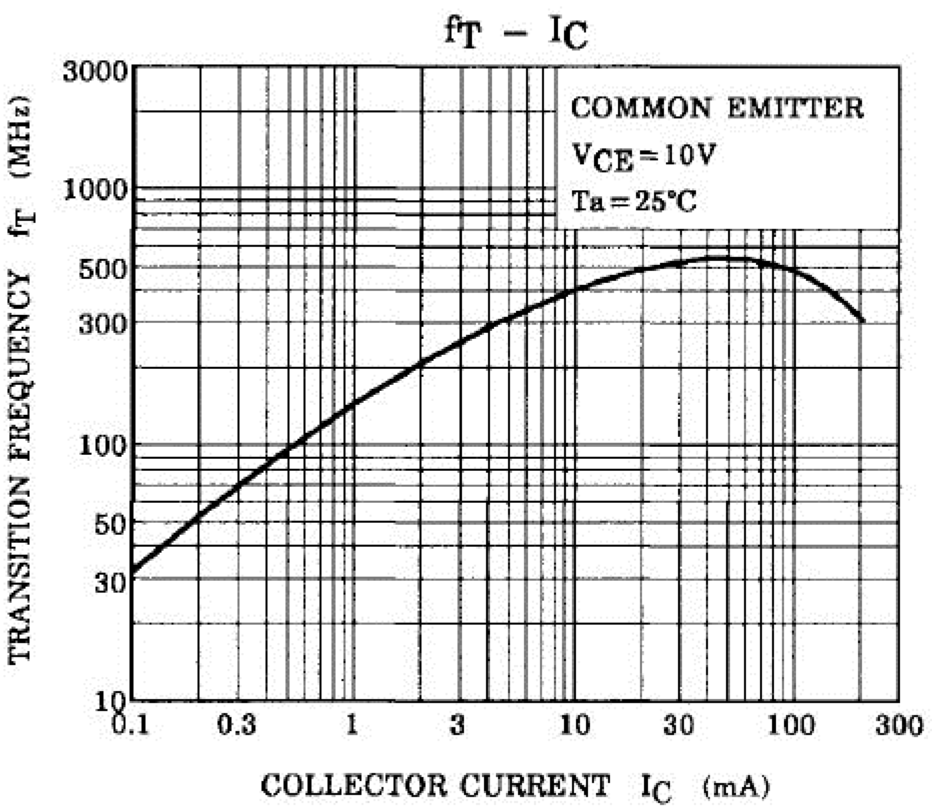
Note: $h_{FE\ (1)}$ classification O: 70~140, Y: 120~240, GR: 200~400, BL: 350~700

Example of transistor datasheet

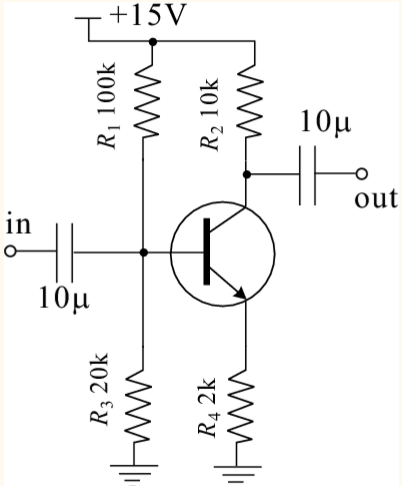


h_{fe} linear model availability in the range of J_C.

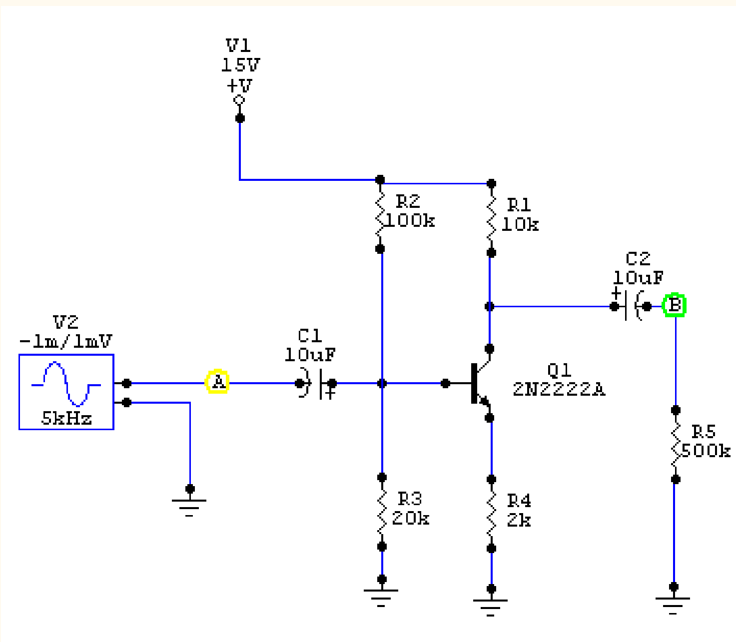
Cut-off frequency as a function of J_C

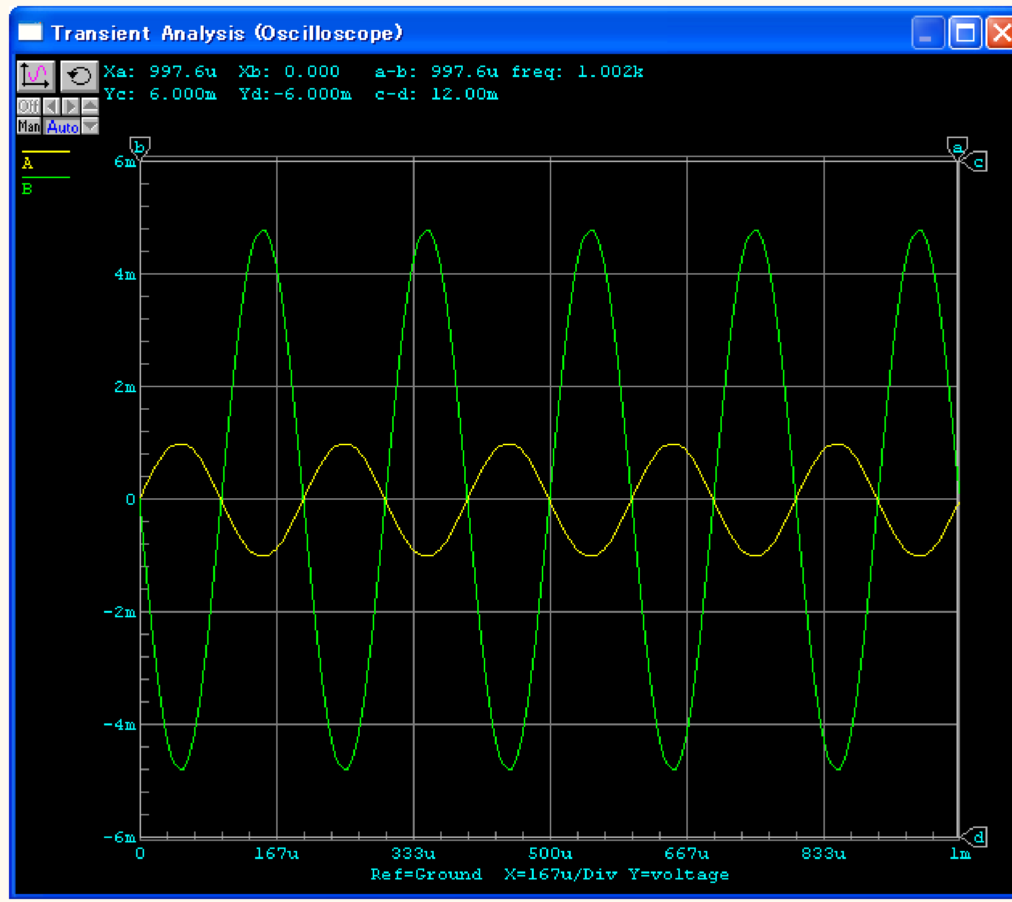


Common emitter (grounded emitter) amplifier circuit



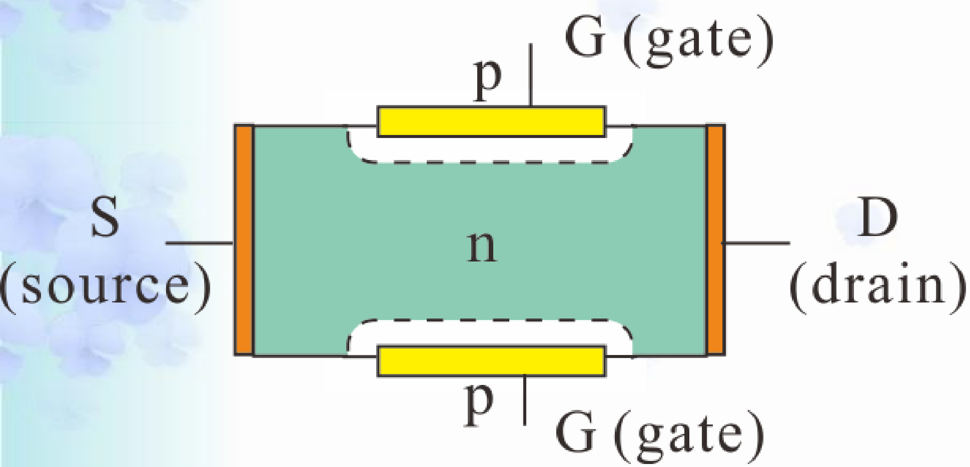
$$\Delta V_{\mathrm{C}} = R_2 \Delta J_{\mathrm{C}} \approx R_2 \Delta J_{\mathrm{E}} = R_2 \frac{\Delta V_{\mathrm{E}}}{R_4} = \frac{R_2}{R_4} \Delta V$$

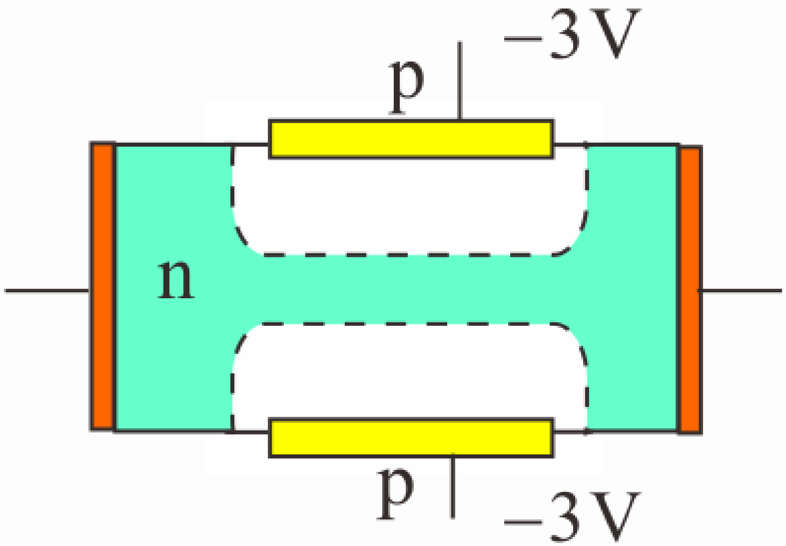




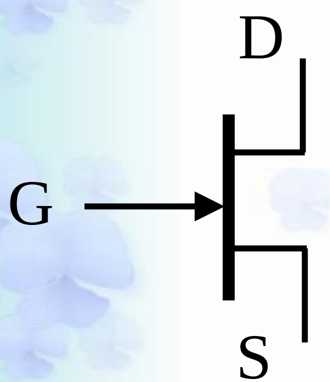
4.4 Field effect transistor (FET)

Junction FET (JFET)

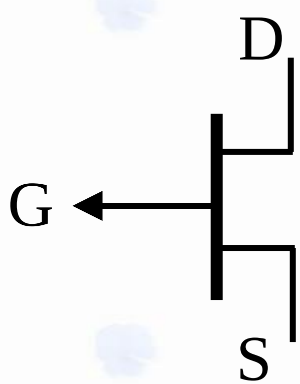




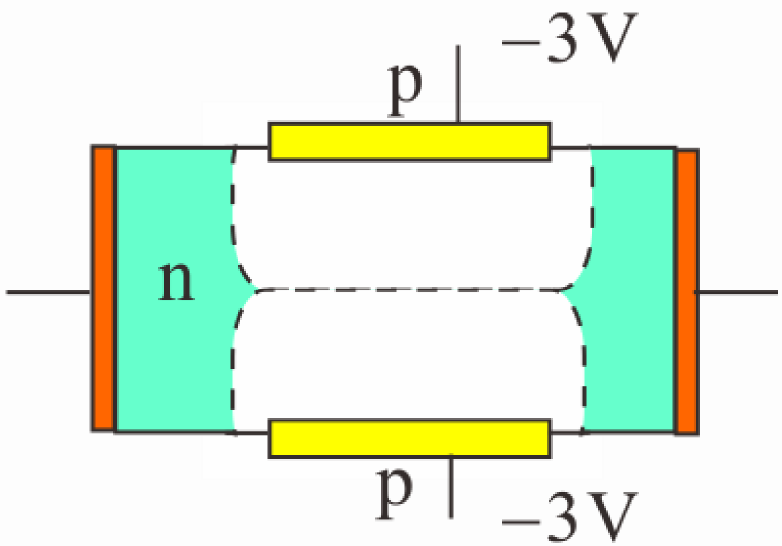
Circuit symbols



n-channel

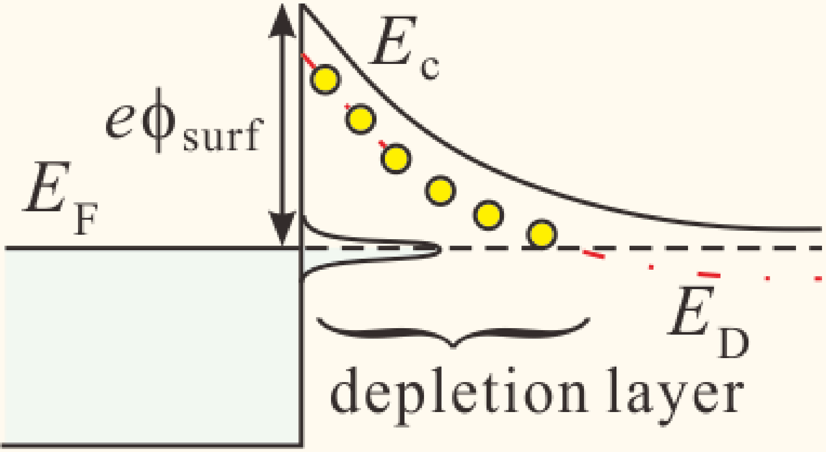


p-channel



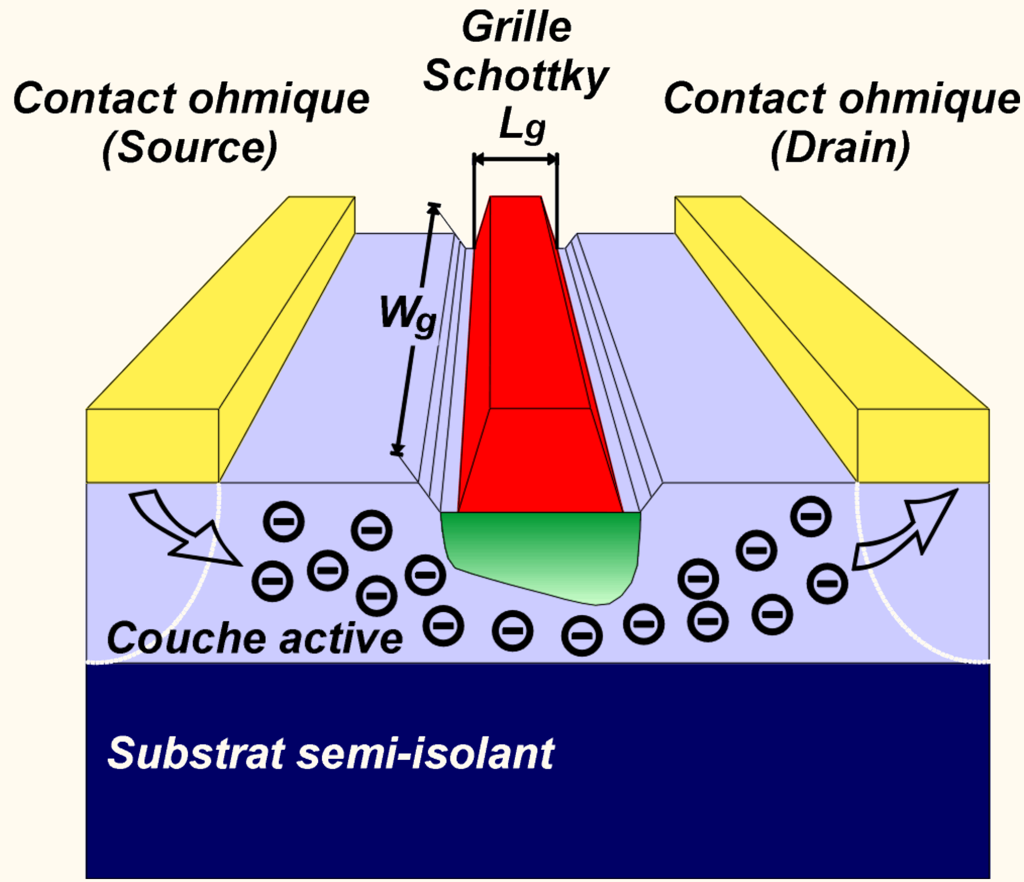
Pinch-off

MES-FET



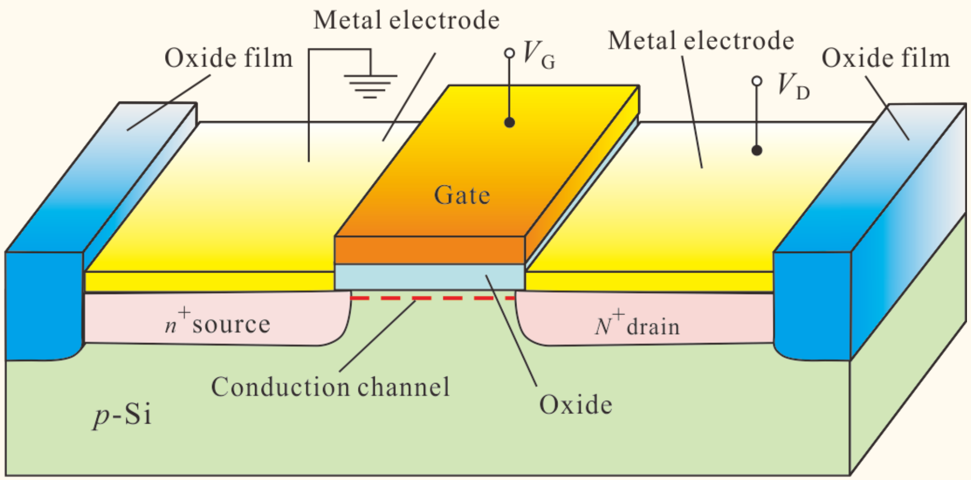
E_c
$e\phi_{surf}$
E_F
E_D
depletion layer

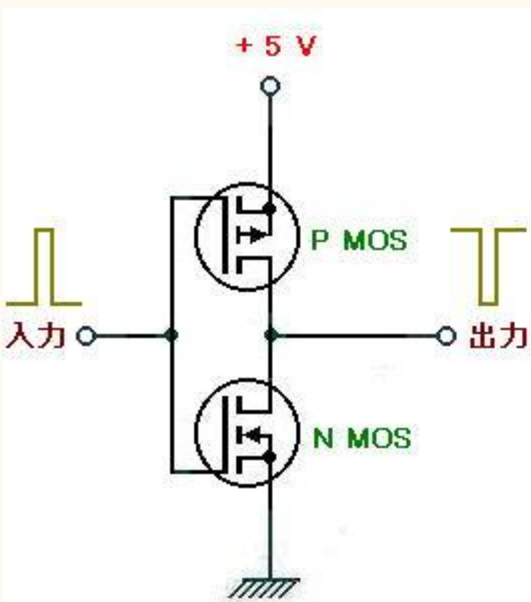
HWS2542
HL8052
HL27



Grille
Schottky
L_g
Contact ohmique
(Source)
Contact ohmique
(Drain)
W_g
Couche active
Substrat semi-isolant

MOS-FET

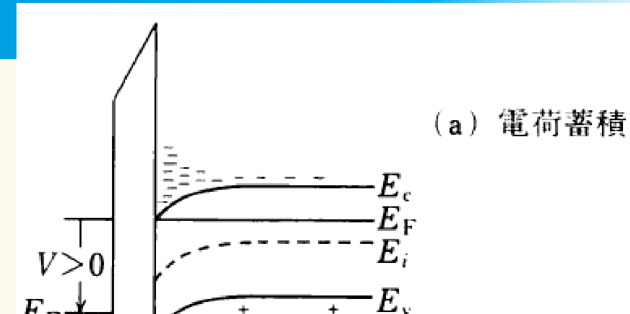




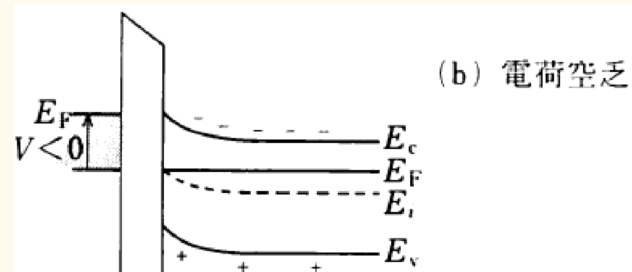
Simplified
CMOS inverter
circuit

Low leakage
current

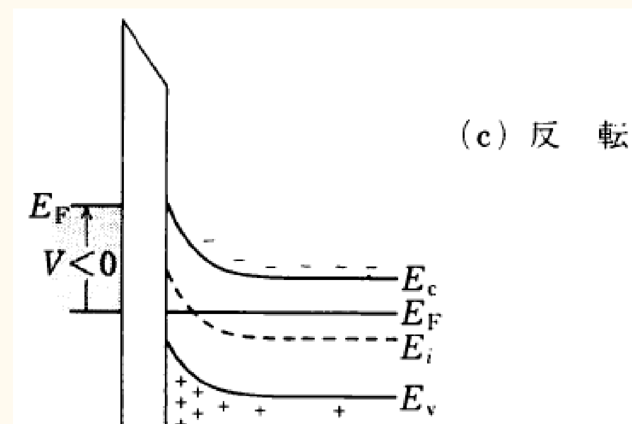
Single gate input
both on/off switch



enhancement

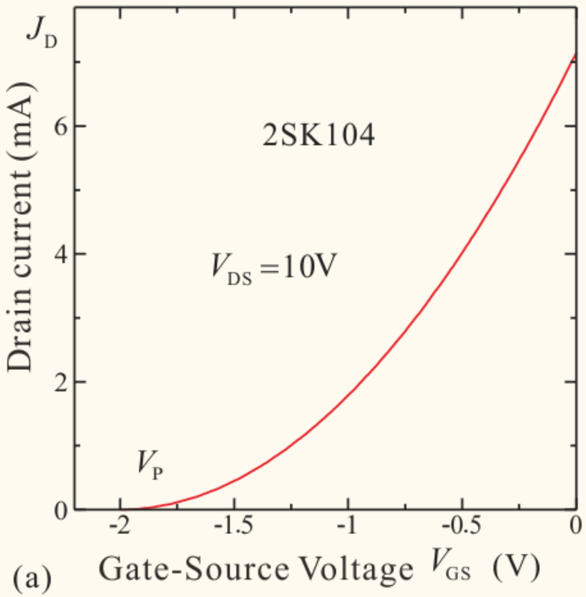


depletion

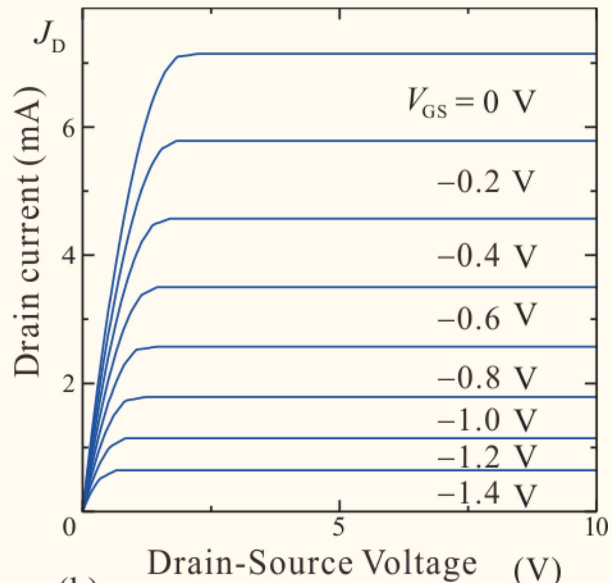


inversion

Static characteristics of FET



(a)



(b)

$$J_G \simeq 0,$$

$$J_D = f(V_G, V_D)$$

$$g_m \equiv \left(\frac{\partial J_D}{\partial V_{GS}} \right)_{V_D = \text{const.}},$$ transconductance

$$r_d \equiv \left(\frac{\partial V_D}{\partial J_D} \right)_{V_{GS} = \text{const.}}$$ Drain resistance

Locally linear approximation $$j_d = g_m v_{gs} + \frac{v_d}{r_d}$$

References

Feedback

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- J. J. Distefano, et al. “Schaum’s outline of theory and problems of feedback and control systems” 2nd ed. (McGraw-Hill, 1990)

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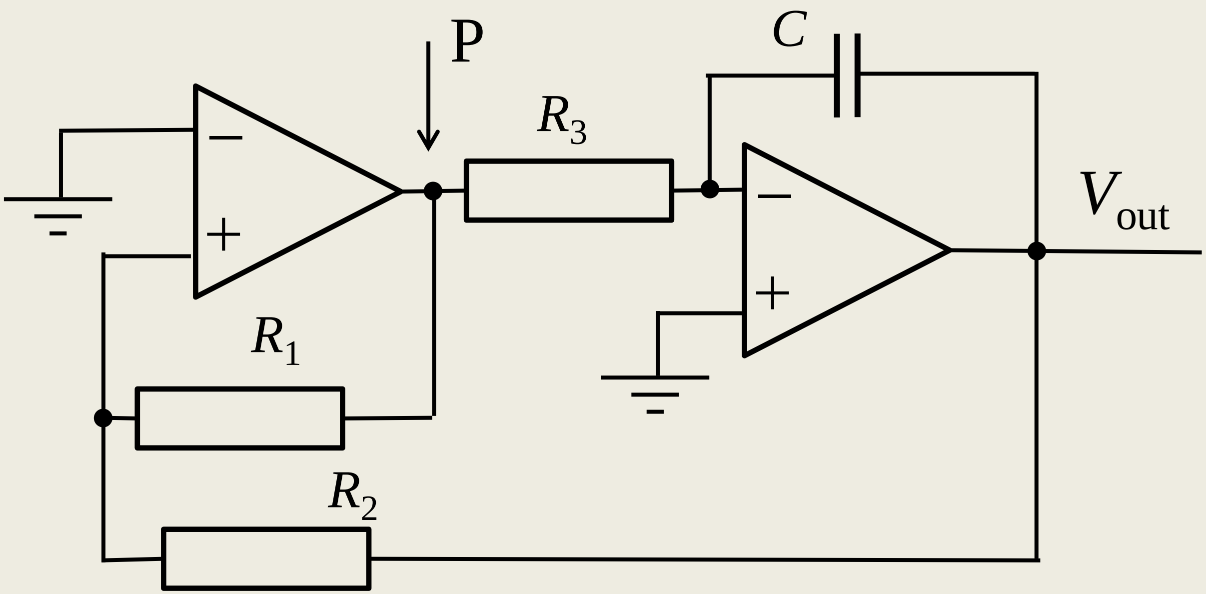
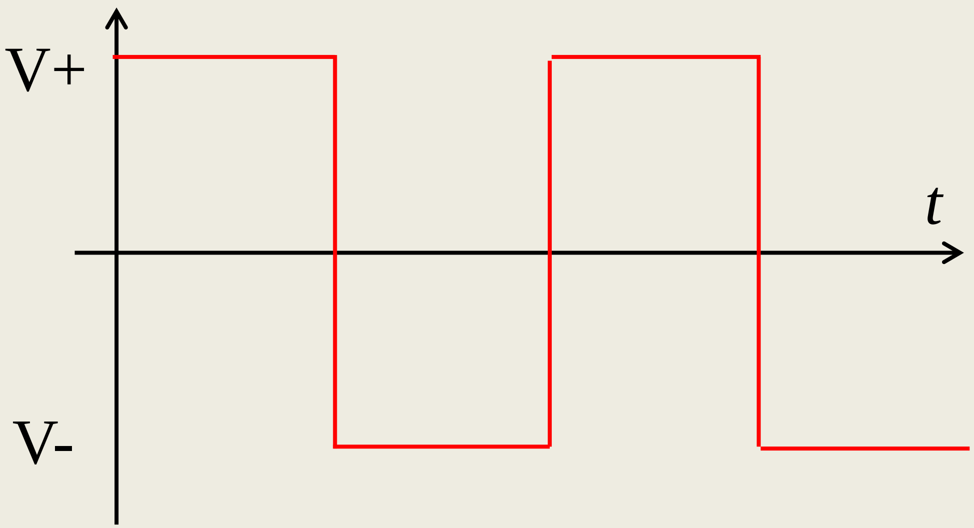
- 岡村迪夫　「OPアンプ回路の設計」　CQ出版社
- J. K. Roberge, K. H. Lundberg, “Operational Amplifiers: Theory and Practice” (MIT, 2007).
  http://web.mit.edu/klund/www/books/opamps181.pdf

BJT, FET circuits

- 松澤昭　「基礎電子回路工学」 (電気学会, 2009).
- S. M. Sze, K. K. Ng, “Physics of Semiconductor Devices” (Wiley, 2007).

Exercise C-1



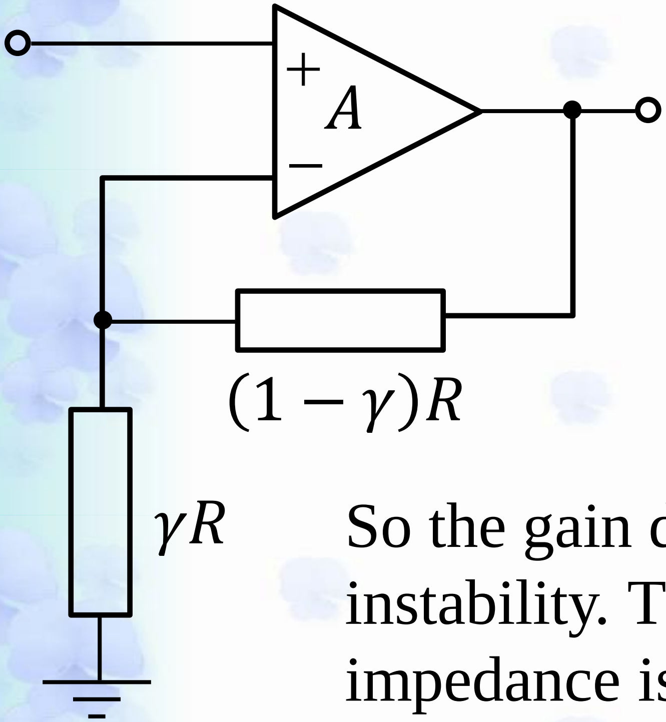


In the circuit shown in the left, at point P, a waveform in the lower panel was observed. Here V+ and V- are power source voltages for + and – respectively.

Draw a rough sketch of the waveform for V_{out}.

"Rough sketch" should contain the levels and the timing of folding points. Write a short comment why V_{out} should be in such a form.

Exercise C-2



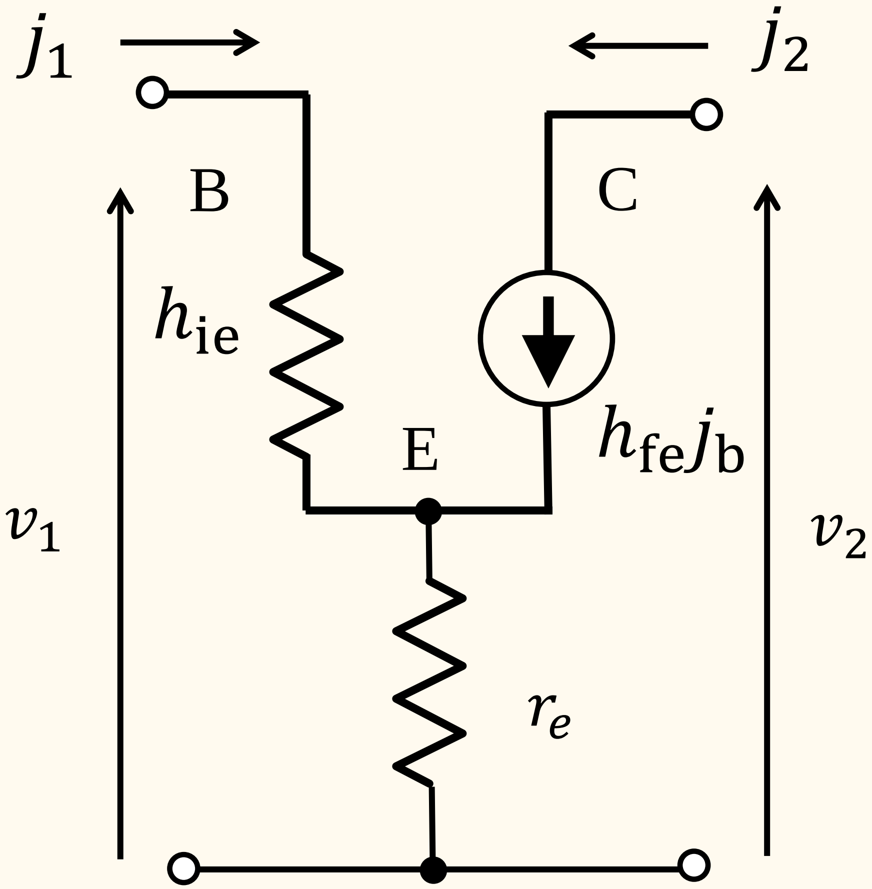
Consider a differential amplifier with the open loop gain

$$A(s) = \frac{A_0\omega_1\omega_2}{s(s+\omega_1)(s+\omega_2)}.$$

So the gain diverges with $s \to 0$ but here we ignore this instability. The input impedance is ∞, and the output impedance is 0.
It is now placed in a circuit with a feedback shown in the left.
Obtain the stability condition for γ.

(hint) Apply the Hurwitz criterion for zeros of even and odd parts of the denominator.
Or just calculate H_2.

Exercise C-3



Let us view a bipolar transistor plus an emitter resistance as a four terminal circuit as shown in the left figure.
Obtain the Y (admittance) matrix defined below for this circuit.

Calculate each element in the Y matrix for
r_e =25Ω, h_{ie} =500 Ω, h_{fe}= 200

$$\begin{pmatrix} j_1 \\ j_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}$$