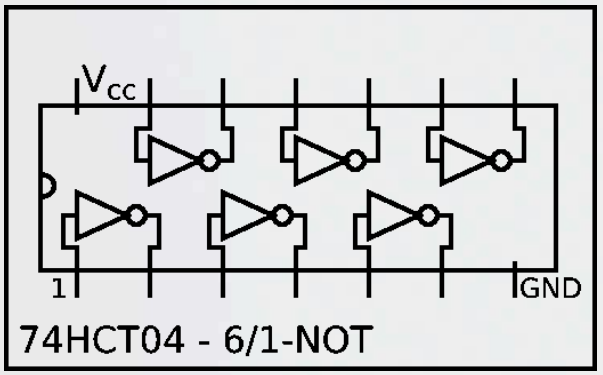
電子回路論第13回 (最終回)
Electric Circuits for Physicists

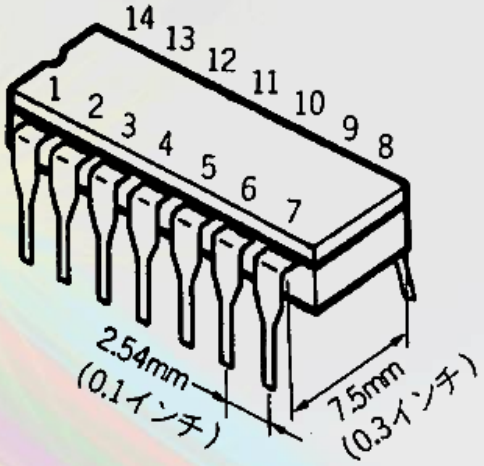
東京大学理学部・理学系研究科
物性研究所
勝本信吾
Shingo Katsumoto

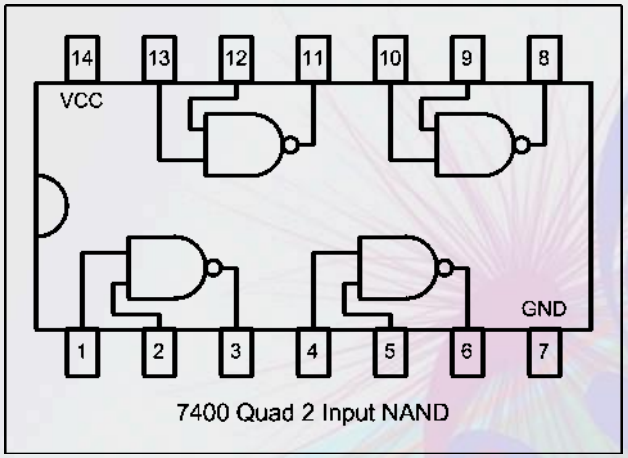
Standard gate logic IC packaging

Full pitch

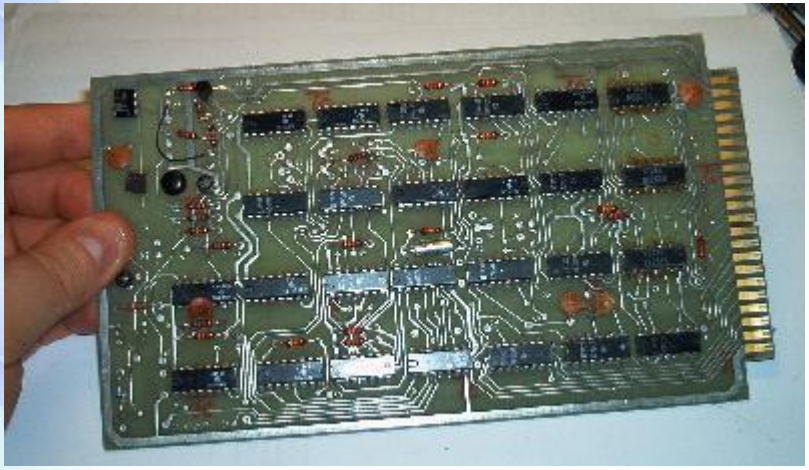
Half pitch surface mount





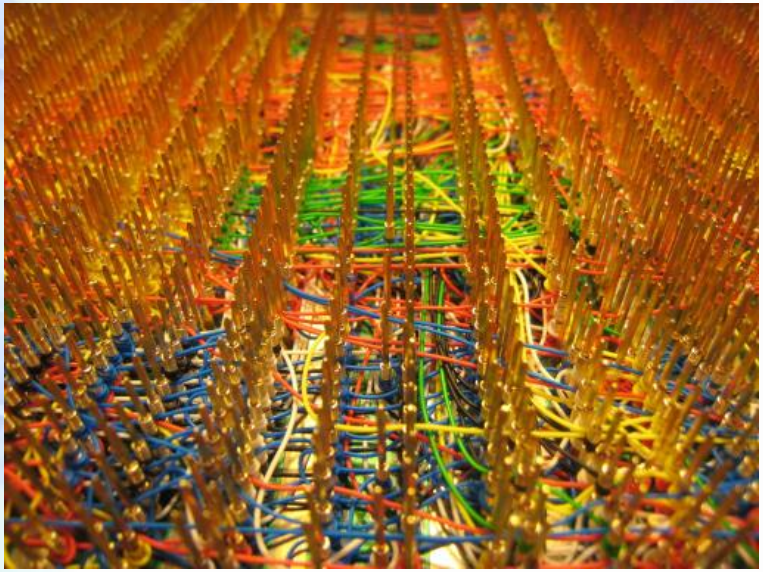


Mounting of logic ICs

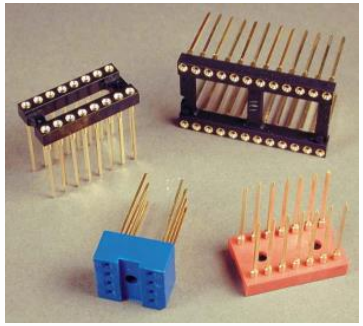


Printed board with soldering

Surface mounting



Wire wrapping



7.5 AD/DA converter circuit

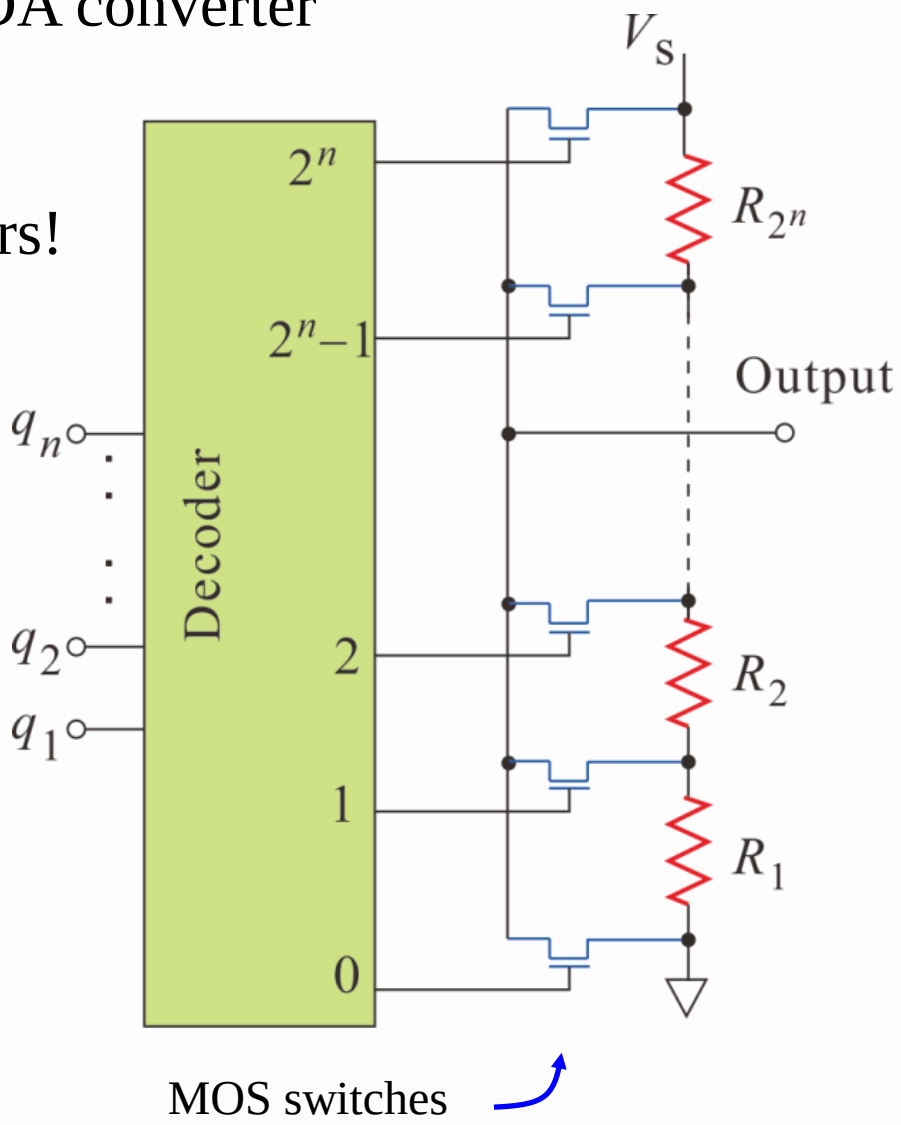
7.5.1 Digital to Analog conversion

Resistor string type DA converter

n bits converter

$\rightarrow 2^n$ outputs!, 2^n resistors!

$$V_{\text{out}} = \frac{p_{\text{input}}}{2^n} V_{\text{S}}$$

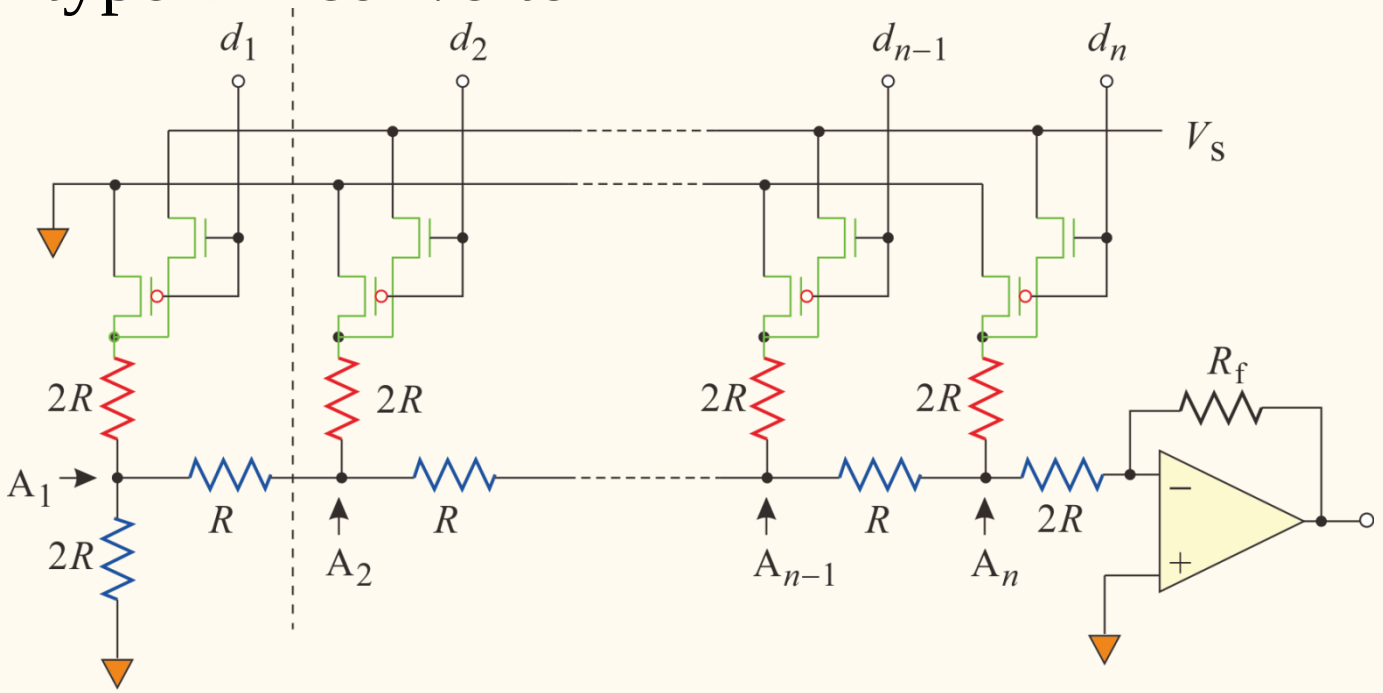


7.5.1 Digital to Analog conversion

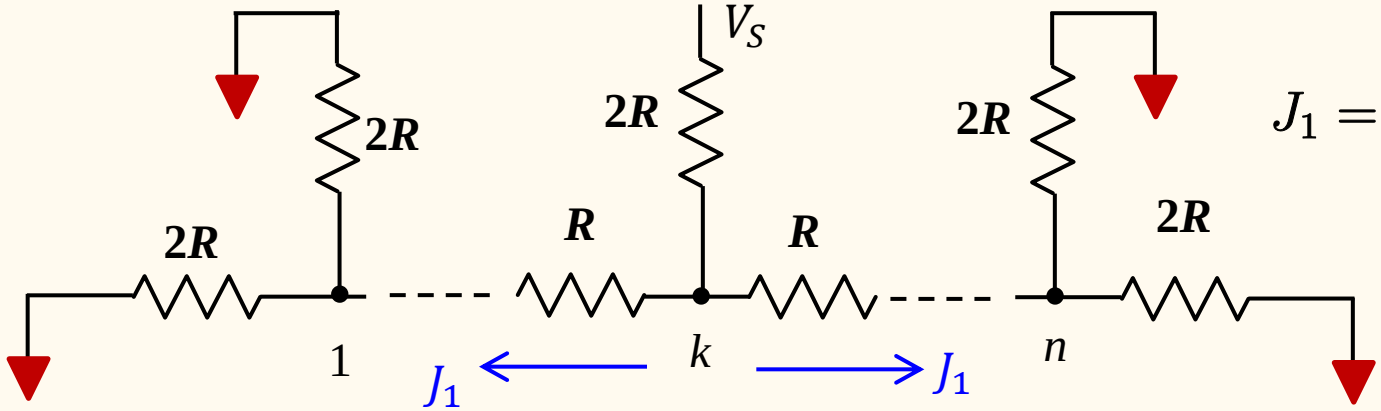
Resistor ladder type DA converter

MOS switch array

ON: V_S
OFF: ground

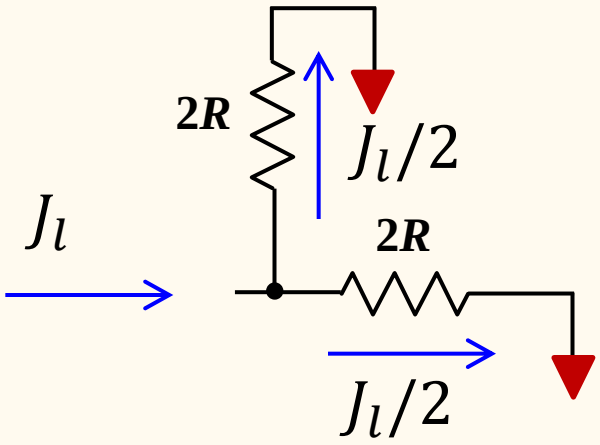


Input $(0,0,\cdots,0,1,0,\cdots,0)$ $\quad d_k = 1$, others = 0

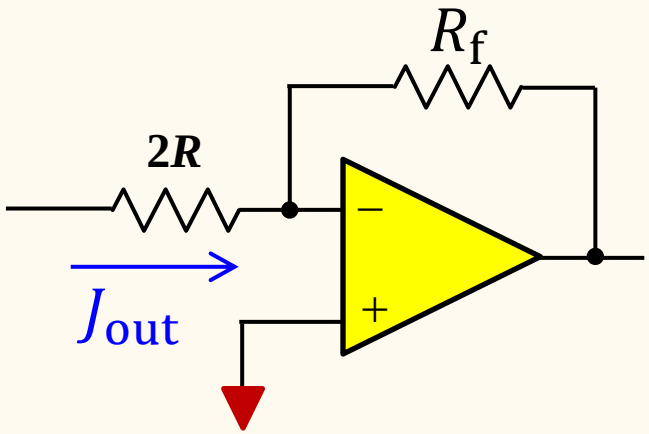


$$J_1 = \frac{V_S}{2 \cdot (2R + R)} = \frac{V_S}{6R}$$

7.5.1 Digital to Analog conversion



$$J_{l+1} = \frac{J_l}{2}$$



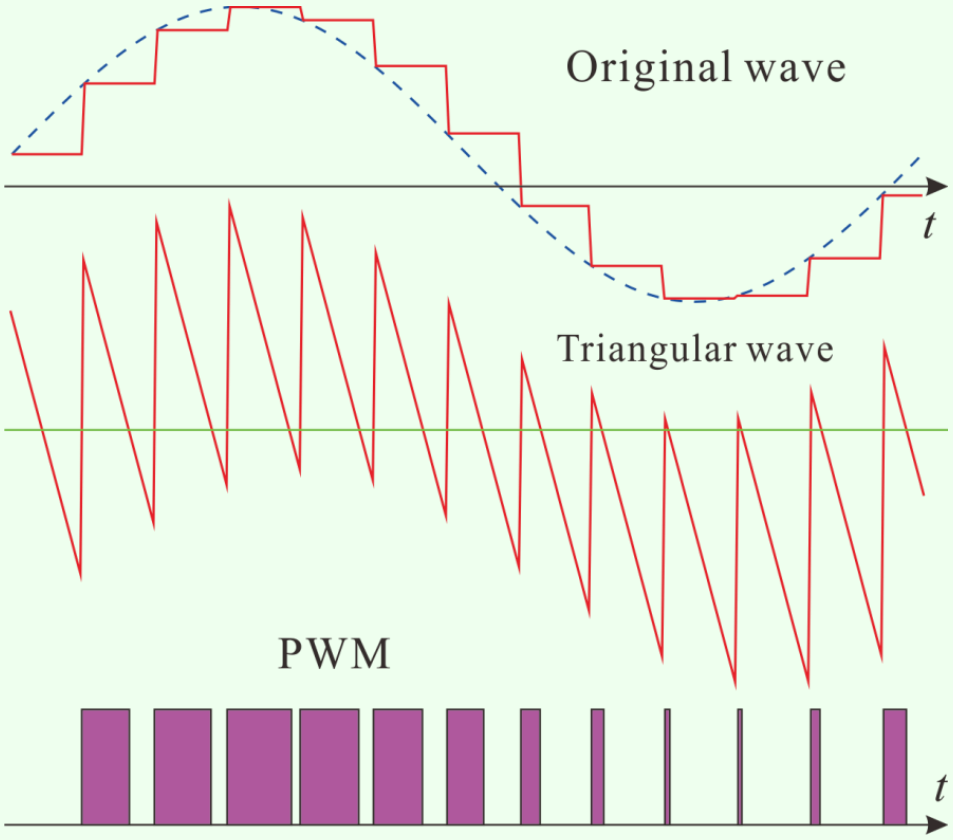
$$J_{\text{out}}(\underset{n}{0\cdots0}\ \underset{k}{1}\ \underset{1}{0\cdots0}) = \frac{V_S}{3R}\left(\frac{1}{2}\right)^{n-k+1} = \frac{V_S}{6\cdot 2^n R}2^k$$

From the superposition theorem:

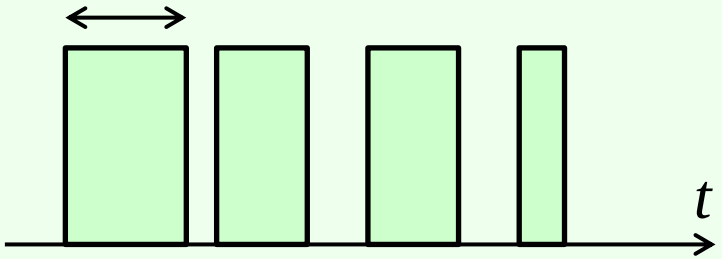
$$V_{\text{out}}(\{d_i\}) = -\frac{1}{3\cdot 2^n}\frac{R_f}{2R}V_S\sum_{k=1}^{n}2^k d_k$$

7.5.1 Digital to Analog converter

Pulse width modulation (PWM)

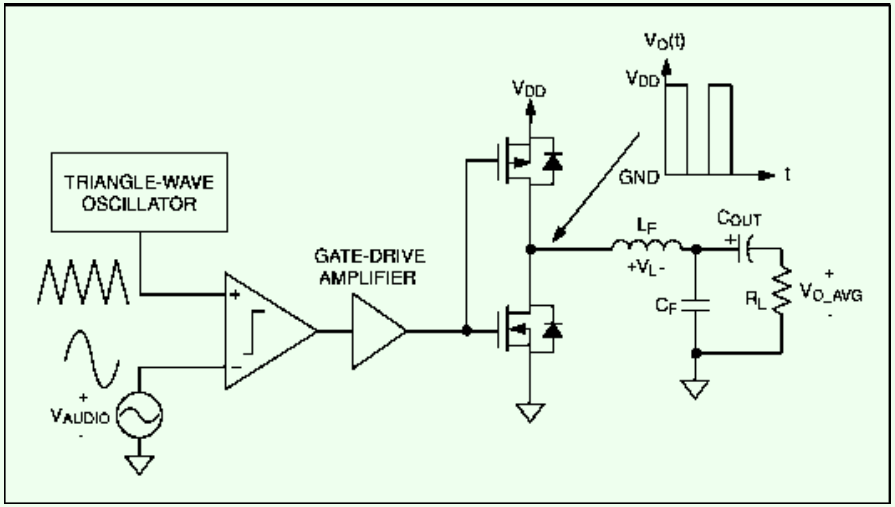


Digital signal →
PWM signal with a counter



Low pass

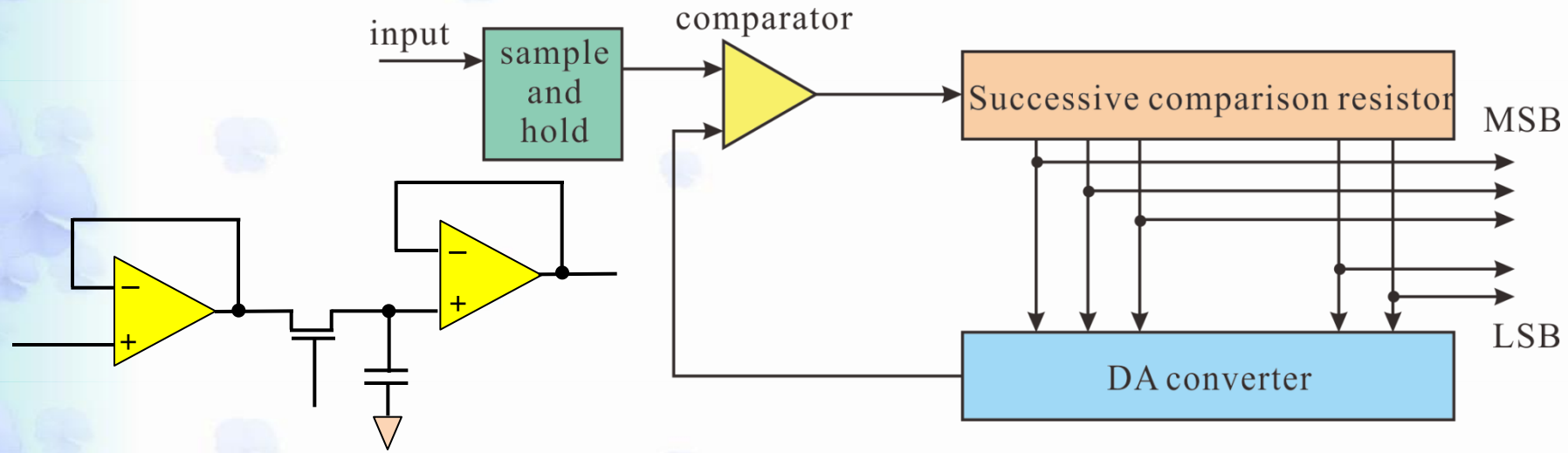
Analog signal



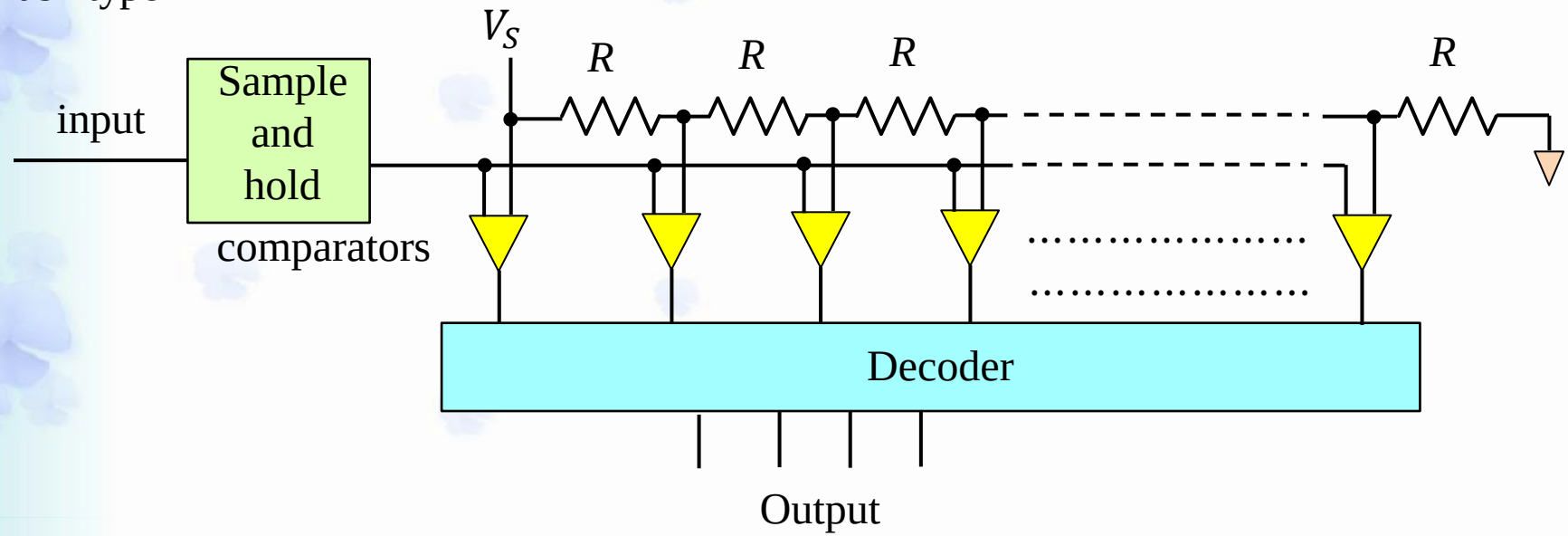
D-class amplifier

7.5.2 Analog-Digital converter

Successive comparison type AD converter

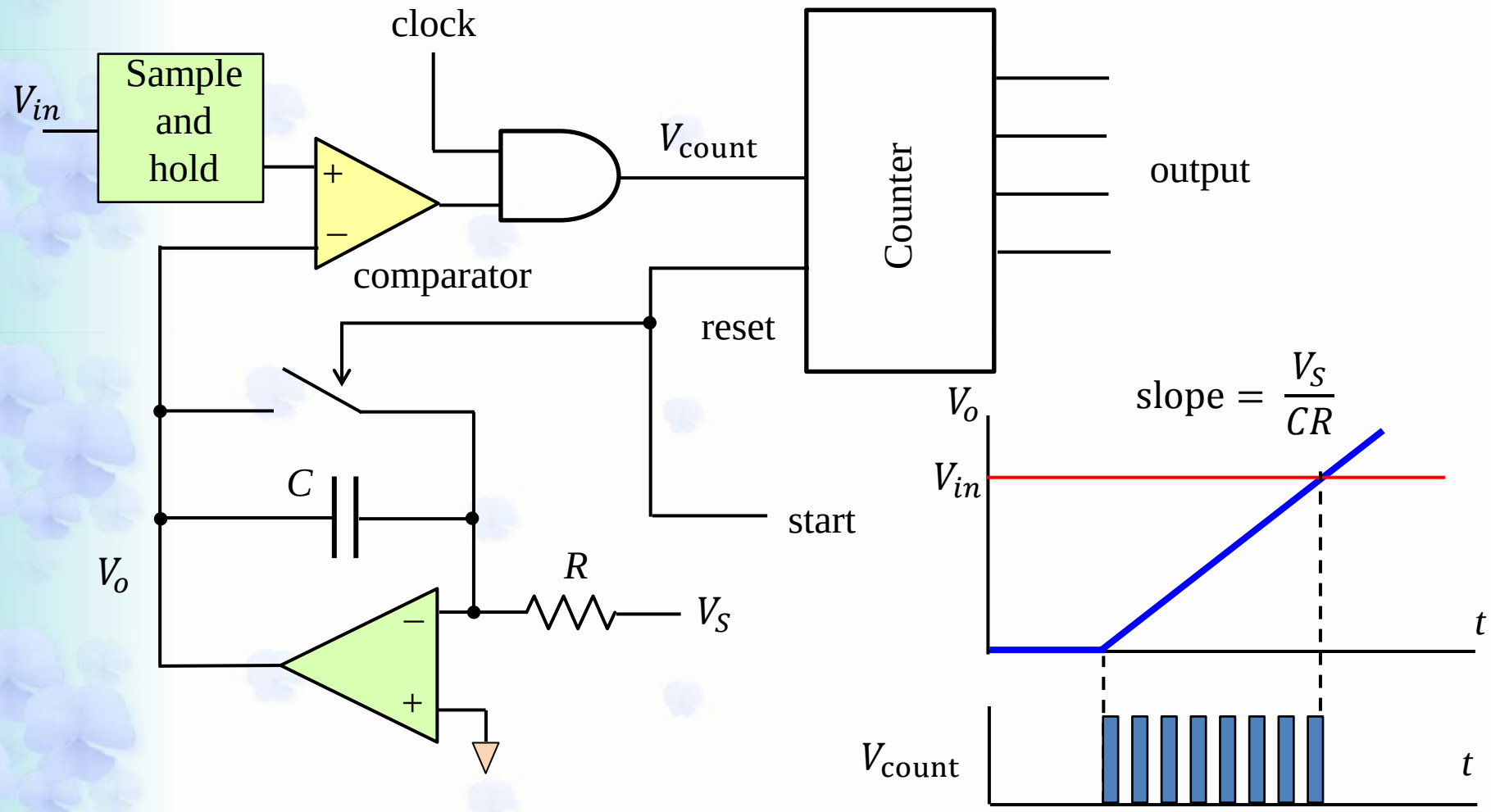


Flush type



7.5.2 Analog-Digital converter

Integrating Analog-Digital Converter



7.6 Digital filter

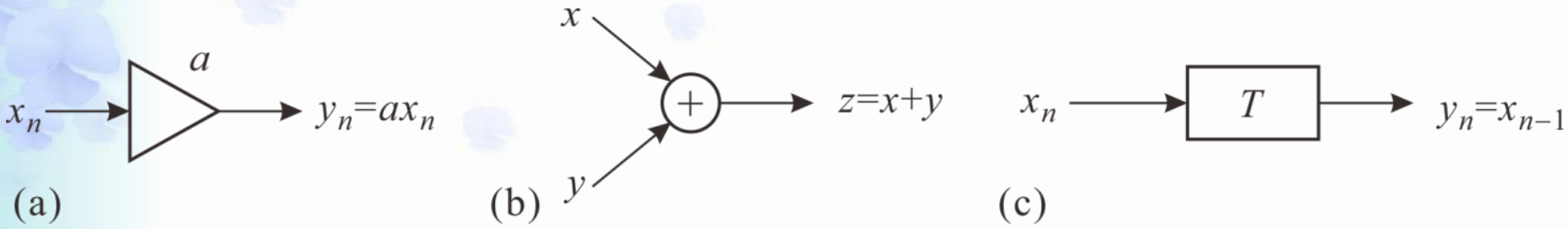
Digital filtering:

$$\{x_i\} = (x_0, x_1, \cdots)$$

$$\{y_i\} = (y_0, y_1, \cdots)$$

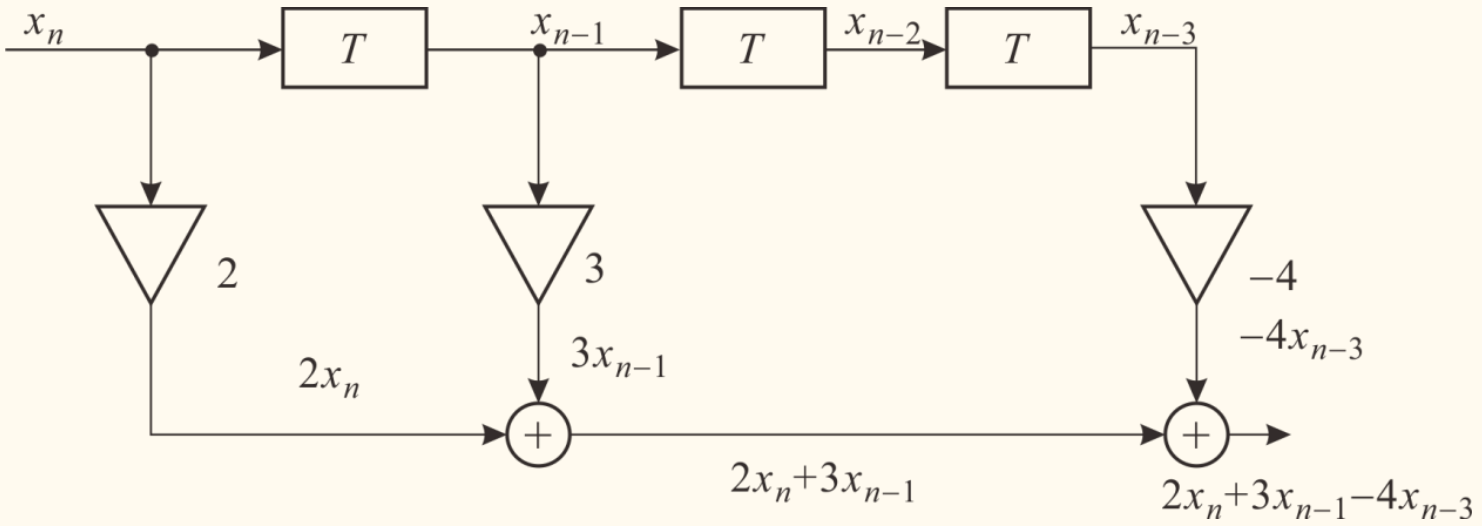
$$y_n = F(x_{n-k}, x_{n-k+1}, \cdots, x_n)$$

Block diagram representation of operations



constant multiplier adder delay (shift resistor)

Block diagram example



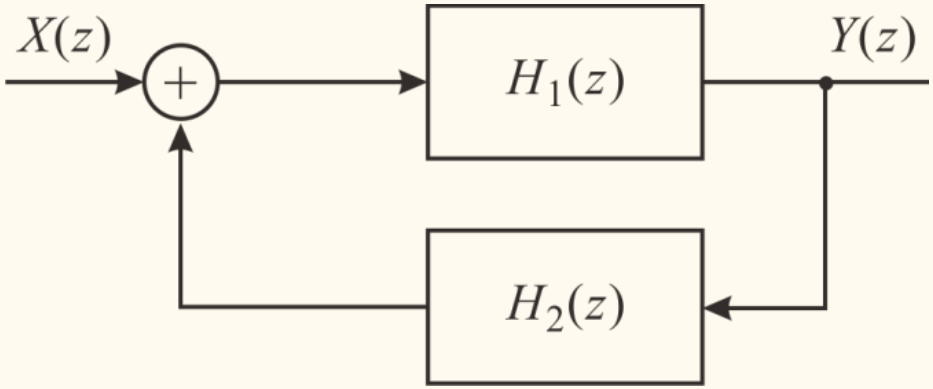
$$y_n = 2x_n + 3x_{n-1} - 4x_{n-3}$$

$$X(z) = \sum_{n=0}^{\infty} x_n z^{-n}, \quad Y(z) = \sum_{n=0}^{\infty} y_n z^{-n}$$

$$\begin{aligned} Y(z) &= 2X(z) + 3z^{-1}X(z) - 4z^{-3}X(z) \\ &= (2 + 3z^{-1} - 4z^{-3})X(z) \end{aligned}$$

$$\therefore H(z) \text{ (transfer function)} = 2 + 3z^{-1} - 4z^{-3}$$

Feedback and transfer function



$$Y(z) = H_1(z)W(z) = H_1(z)(X(z) + H_2(z)Y(z)),$$

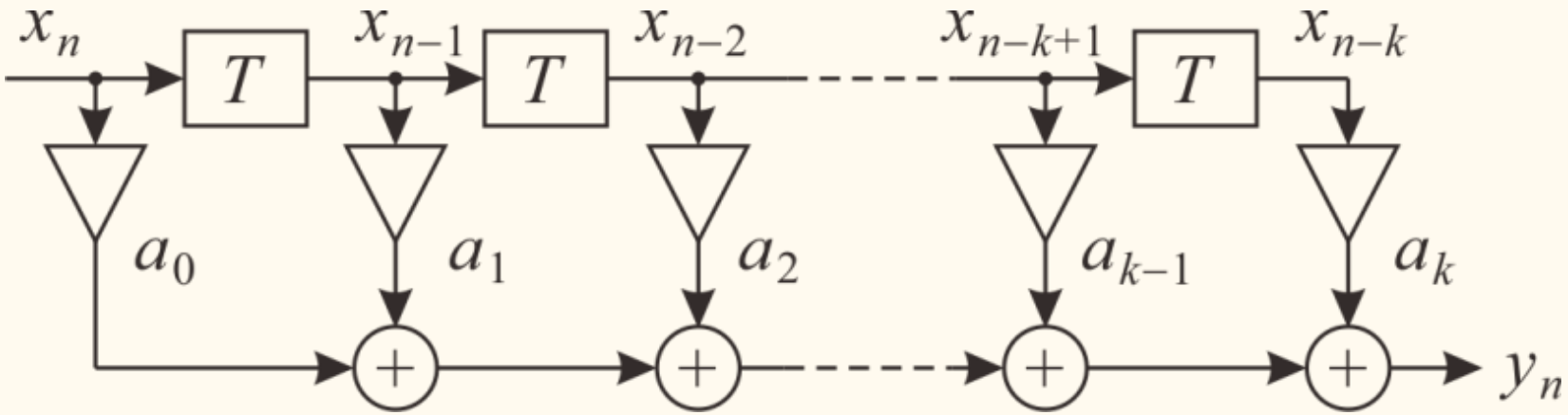
$$\therefore Y(z) = \frac{H_1(z)}{1 - H_1(z)H_2(z)}X(z)$$

$$H(z) = \frac{H_1(z)}{1 - H_1(z)H_2(z)}$$

$$(\text{transfer function}) = \frac{(\text{direct gain})}{1 - (\text{feedback transfer gain})}$$

FIR filter

Finite impulse response (FIR) filter

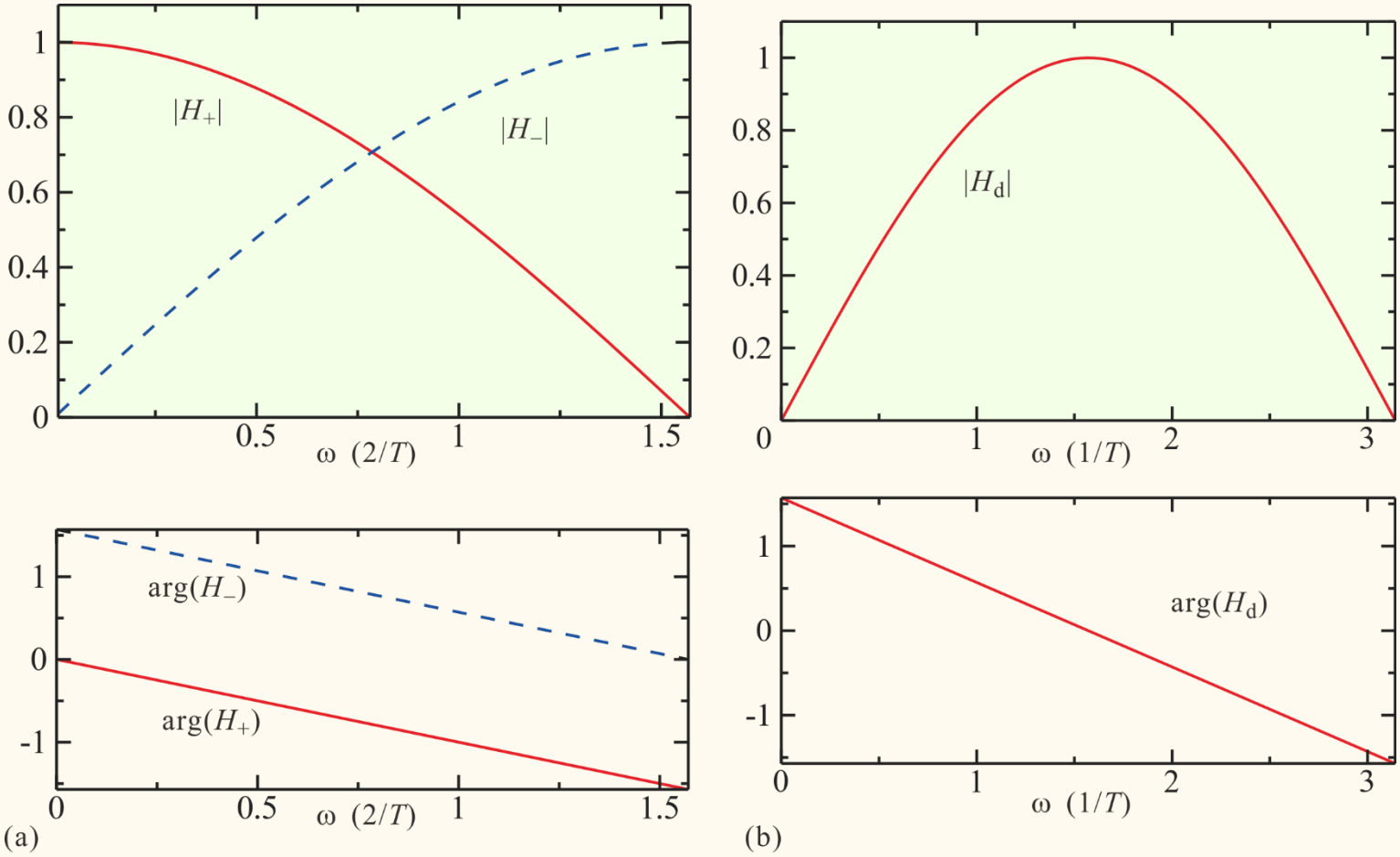


$$H(e^{i\omega\tau}) = \sum_{j=0}^{k} a_j e^{-ij\omega\tau}$$

A Simple example of FIR filter

Moving average, differentiation: $F_{\pm}(x_n, x_{n-1}) = (x_n \pm x_{n-1})/2$

$$H_{\pm}(e^{i\omega\tau}) = e^{-i\omega\tau/2} \begin{pmatrix} \cos(\omega\tau/2) \\ i\sin(\omega\tau/2) \end{pmatrix}$$

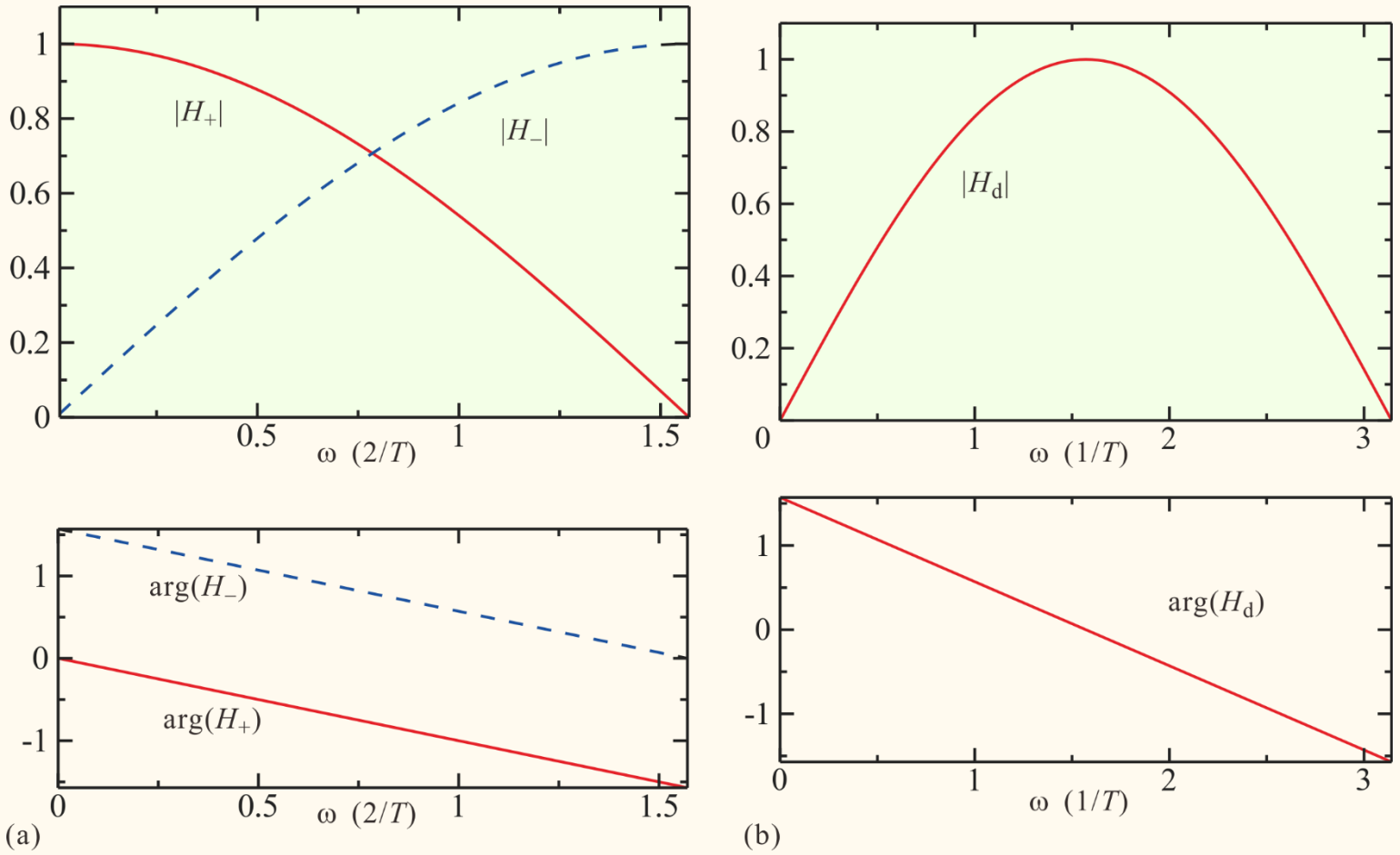


A Simple example of FIR filter

Differentiation of moving average:

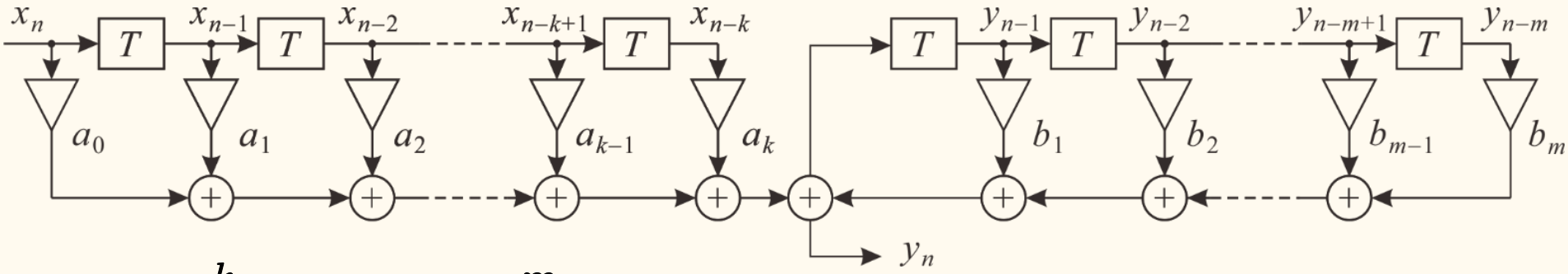
$$F_{\mathrm{d}} = [(x_n + x_{n-1}) - (x_{n-1} + x_{n-2})]/2 = [x_n - x_{n-2}]/2$$

$$H_{\mathrm{d}} = (1 - e^{-2i\omega\tau})/2 = ie^{-i\omega\tau} \sin \omega\tau$$



IIR Filter

Infinite impulse response (IIR) filter:



$$y_n = \sum_{l=0}^{k} a_l x_{n-l} + \sum_{j=1}^{m} b_j y_{n-j}$$

Stability condition: $\lim_{n\to\infty} y_n = 0$

$$Y(z) = X(z)\sum_{l=0}^{k} a_l z^{-l} + Y(z)\sum_{j=1}^{m} b_j z^{-j}$$

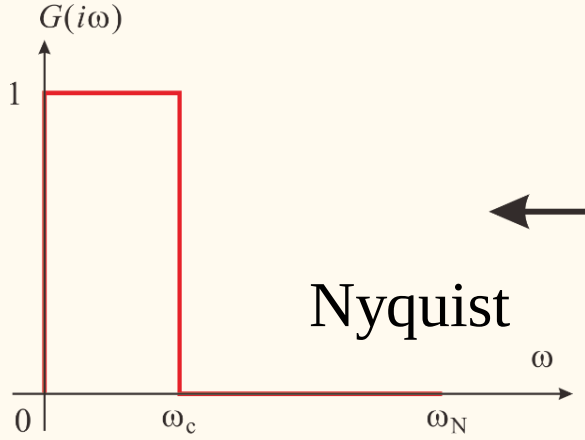
$$H(z) = \frac{Y(z)}{X(z)} = \sum_{l=0}^{k} a_l z^{-l} \Bigg/ \left(1 - \sum_{j=1}^{m} b_j z^{-j}\right)$$

Conversion of z-transform: $|z| > 1$ the poles should be in $|z| < 1$

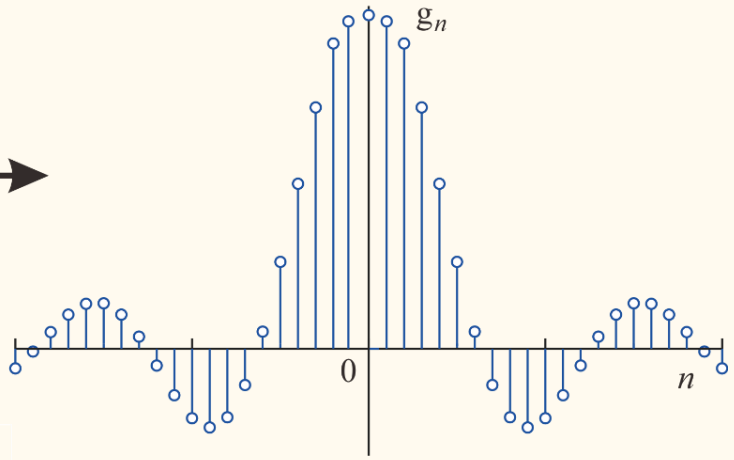
Design of FIR filter: Window function

Ideal low pass filter $G(e^{i\omega\tau}) = \begin{cases} 1, & |\omega| \le \omega_c, \\ 0, & \omega_c < |\omega| \le \omega_N \text{ Nyquist frequency} \end{cases}$

$$G(e^{i\omega\tau}) = \frac{\omega_c}{\omega_N} \sum_{n=-\infty}^{\infty} \frac{1}{n\pi} \mathrm{sinc}\left(n\frac{\omega_c}{\omega_N}\right) e^{-ni\omega\tau} = \gamma_c \sum_{n=-\infty}^{\infty} \frac{1}{n\pi} \mathrm{sinc}(n\gamma_c) z^{-n}$$



Nyquist



Cut the series at a finite number

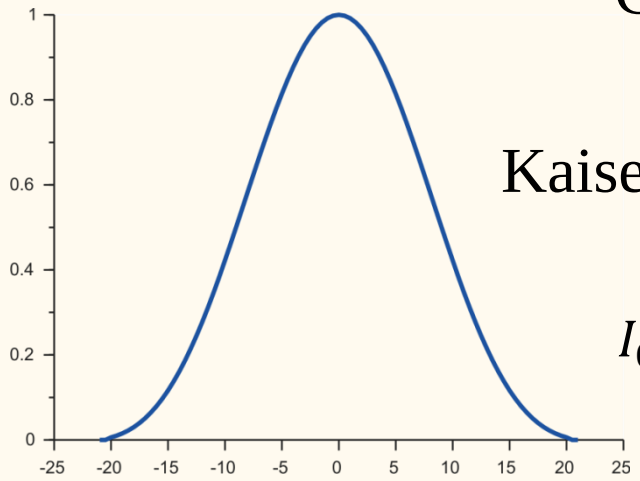
$n_{\mathrm{cut}} = 20$

Ripples in frequency characteristics

Design of FIR filter: Window function

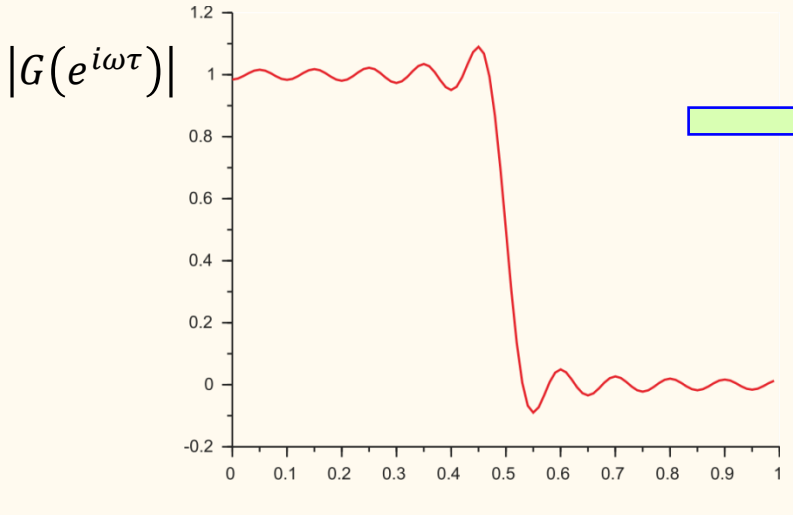
Sudden cutting of z-transform series → Ripples

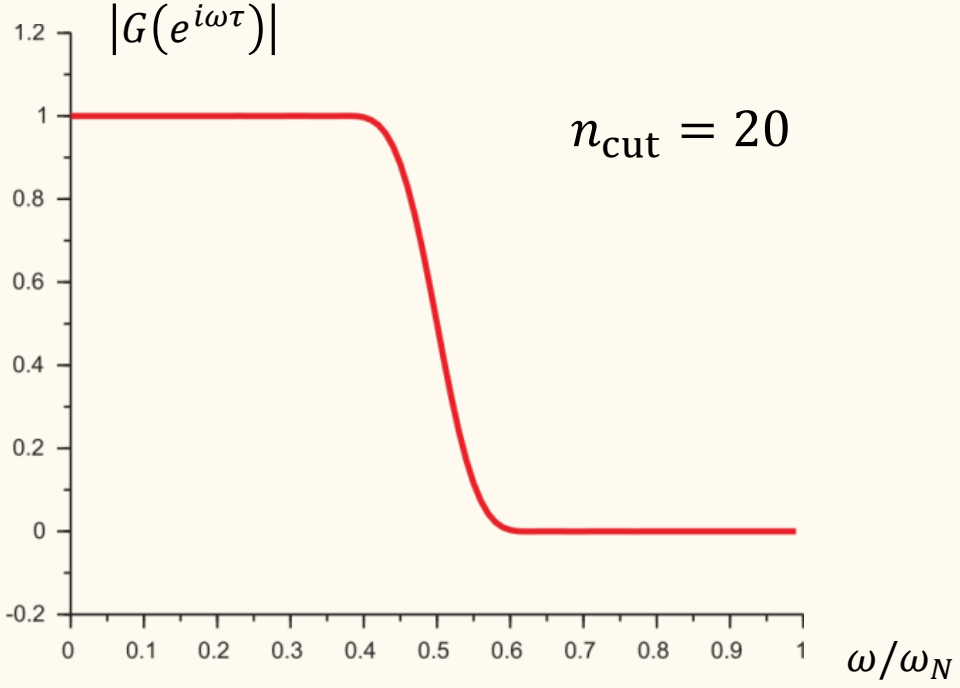
Cut with a smooth function



Kaiser window $w_n = \begin{cases} \dfrac{I_0\left(\alpha\sqrt{1-(n/L)^2}\right)}{I_0(\alpha)} & |n| \le L, \\ 0 & |n| > L \end{cases}$

I_0 : 0th order 1st type modified Bessel function





Design of IIR filter

Transfer function: a rational function (有理式)

A way to design IIR filter: modification of analog filter transfer function

Remember: Butterworth filter

$$\Xi(s) = \sum_{k=0}^{N-1} \frac{\omega_k}{s - s_k}, \qquad s_k = r_c \exp\left[i \left\{ \frac{\pi}{2} + \frac{(2k+1)\pi}{2n} \right\} \right]$$

$$\xi(t) = u_{\mathrm{H}}(t) \sum_{k=0}^{n-1} w_k \exp(s_k t)$$

Heaviside function

$$h_n = h_{\mathrm{H}n} \sum_{k=0}^{n-1} w_k e^{n s_k},$$

Time discretization with $\tau = 1$:

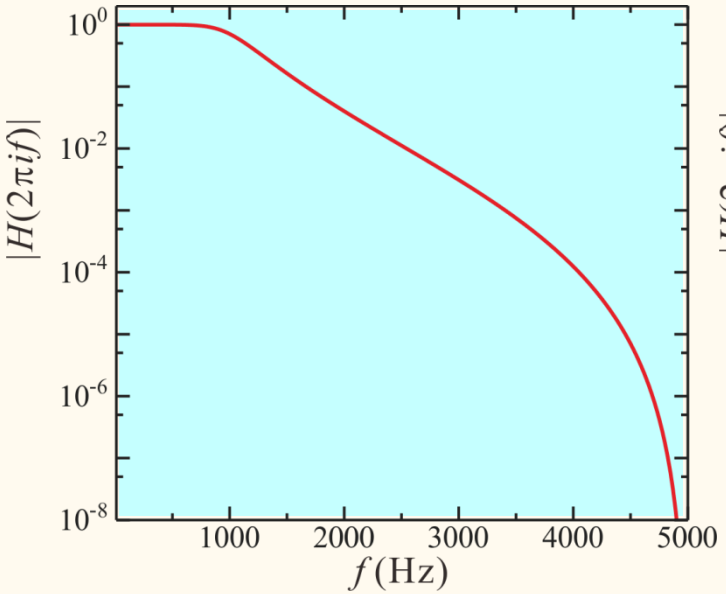
$$\therefore H(z) = \sum_{k=0}^{n-1} \frac{w_k}{1 - \exp(s_k) z^{-1}}$$

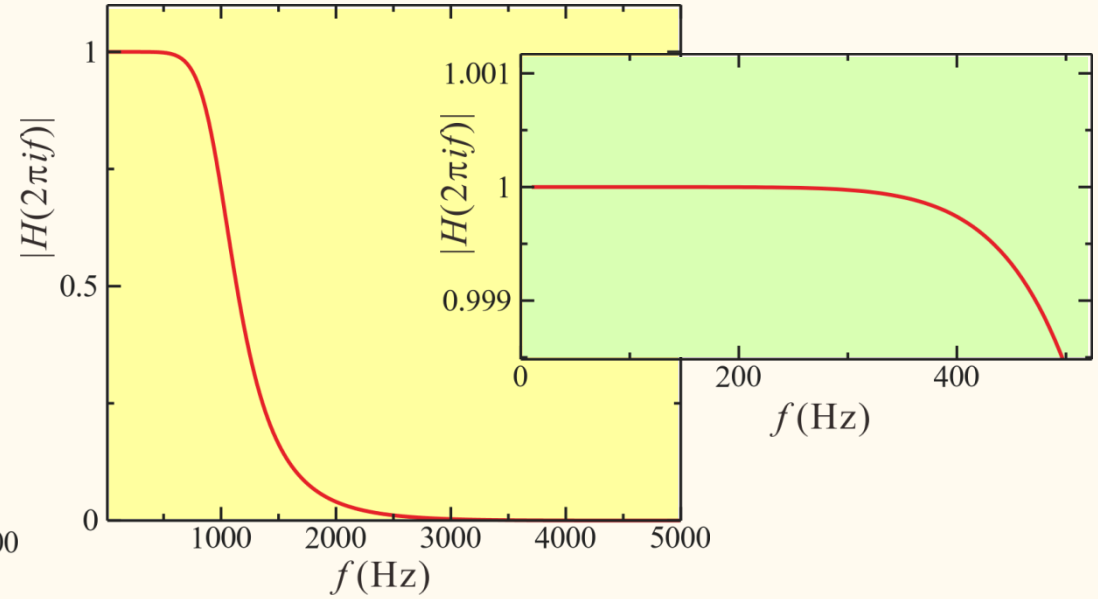
Design of IIR filter

Impulse invariant method: $$\frac{1}{s - s_k} \rightarrow \frac{1}{1 - \exp(s_k) z^{-1}}$$

Bilinear z-transform (双一次z变换法) : $$s \rightarrow \frac{1 - z^{-1}}{1 + z^{-1}}$$

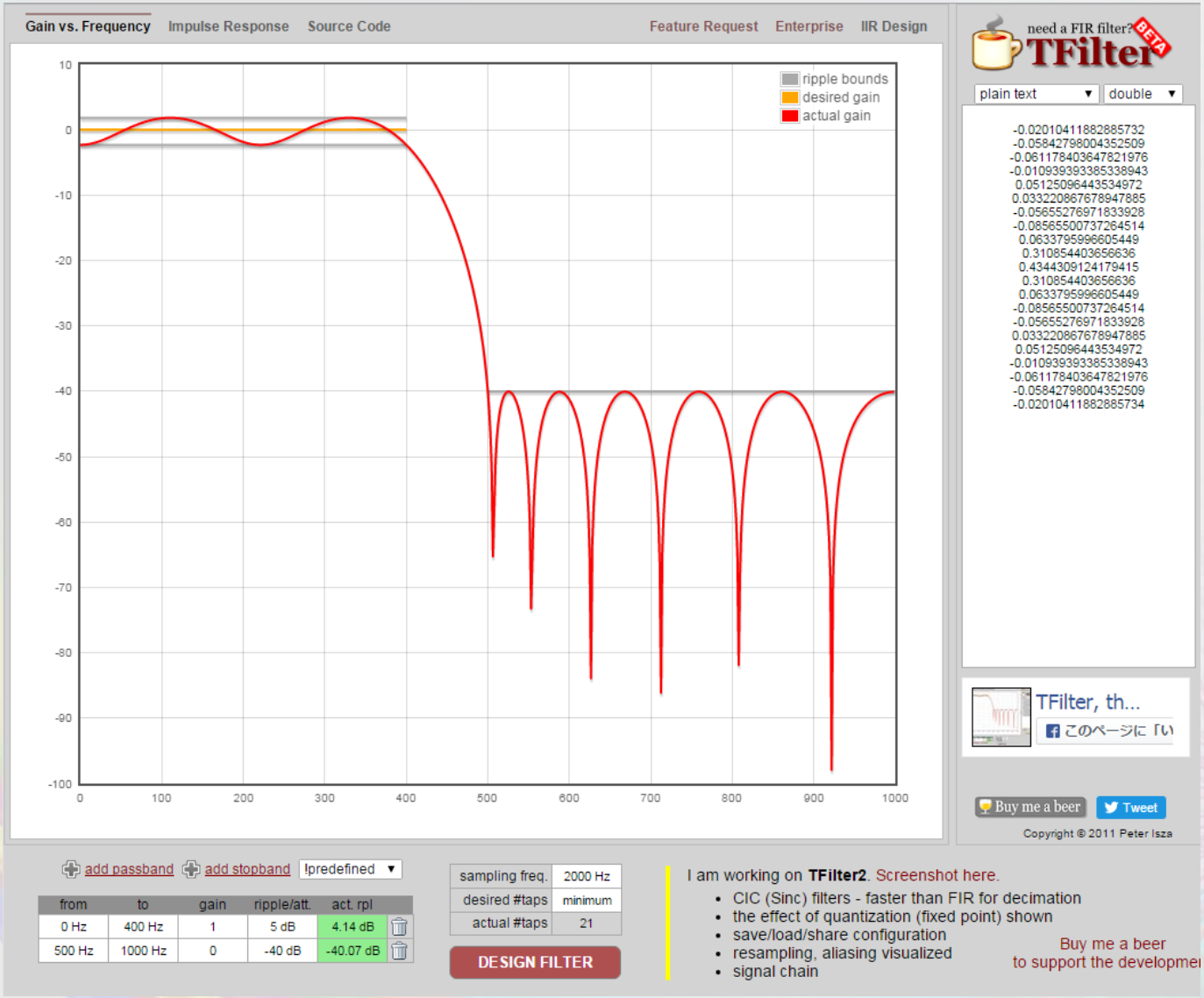
4th Butterworth: $$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4}}{1 - a_1 z^{-1} - a_2 z^{-2} - a_3 z^{-3} - a_4 z^{-4}}$$





Digital filter design web application

http://t-filter.engineerjs.com/



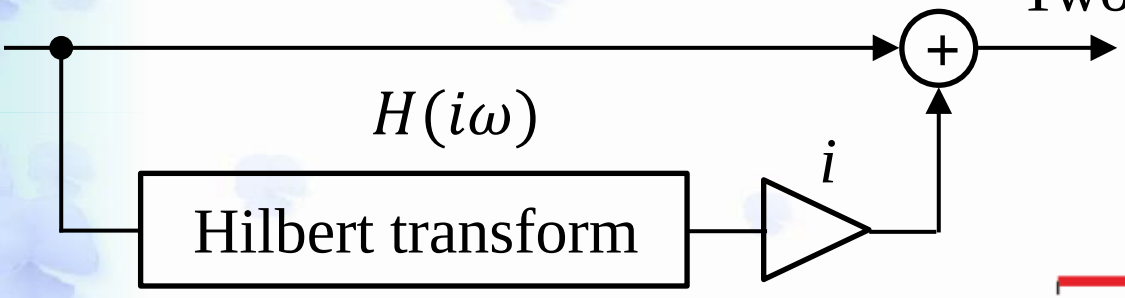
Transferring signal into complex number

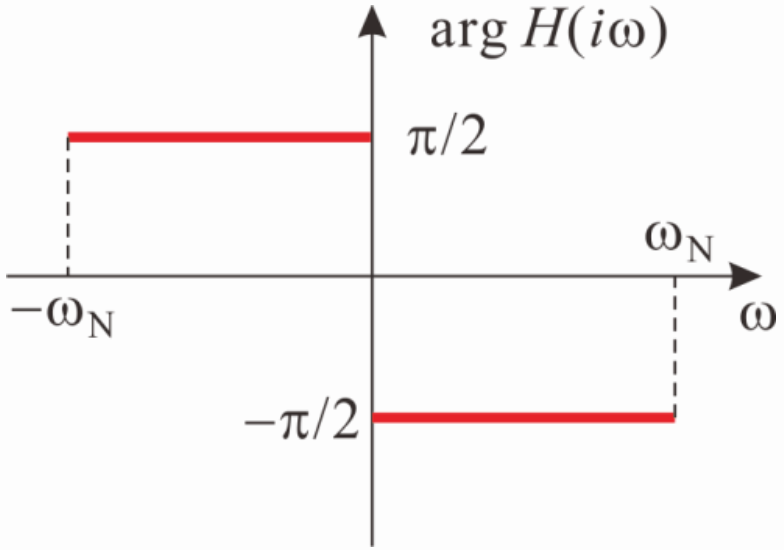
Making complex signal:

$$\cos(\omega t + \theta_0) \;\rightarrow\; \exp[i(\omega t + \theta_0)] = \cos(\omega t + \theta_0) + i\sin(\omega t + \theta_0)$$

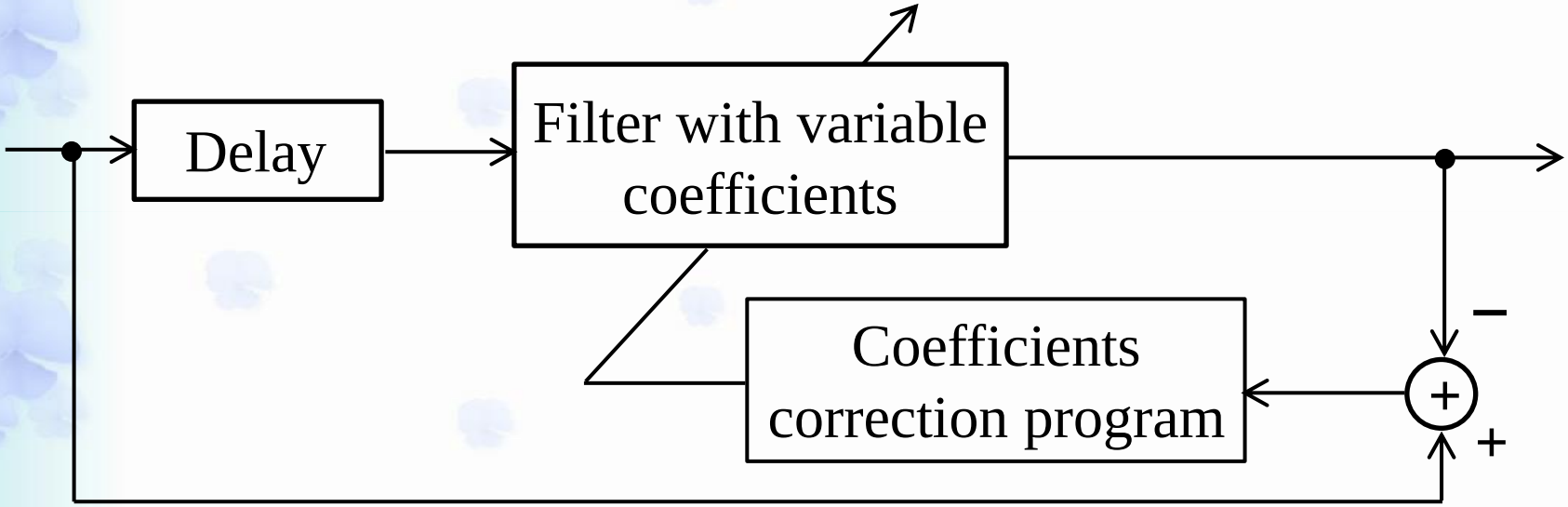
$-\pi/2$ phase shift

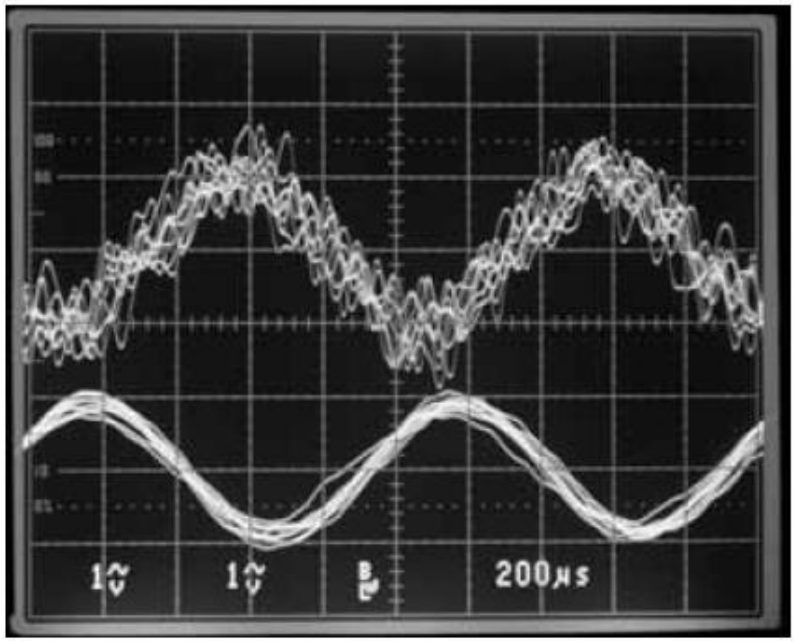
Two-dimensional signal



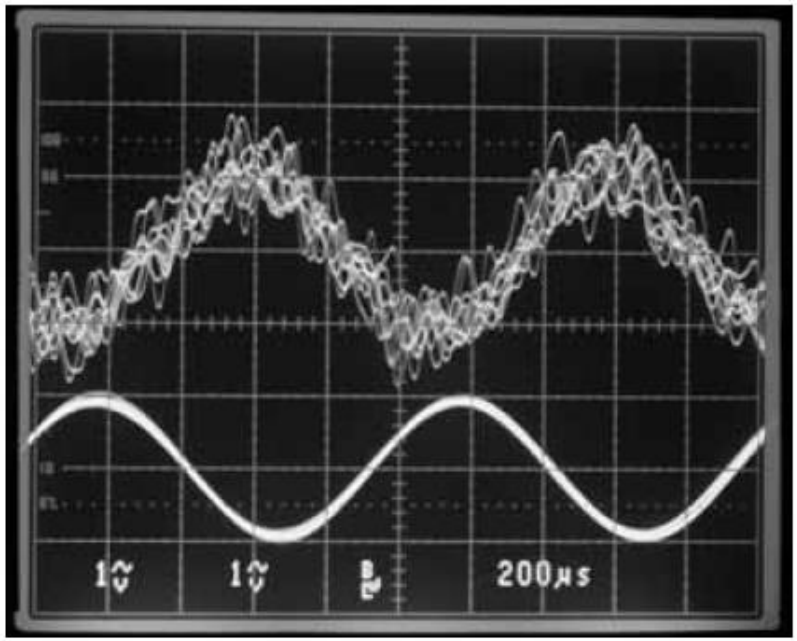


Adaptive filter





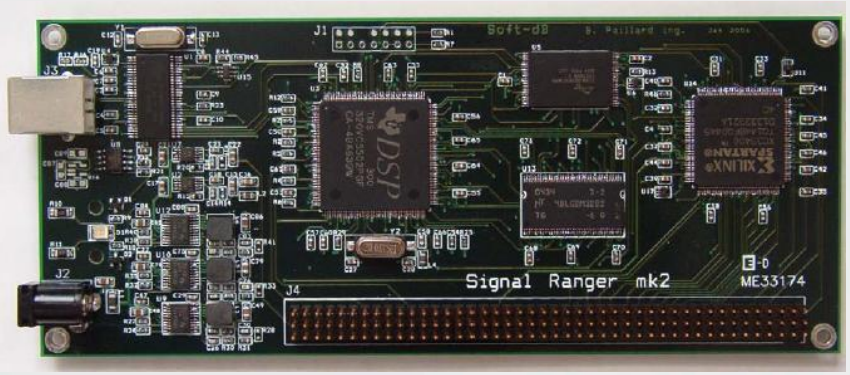
(a) $\mu = 1 \times 10^{-3}$の場合

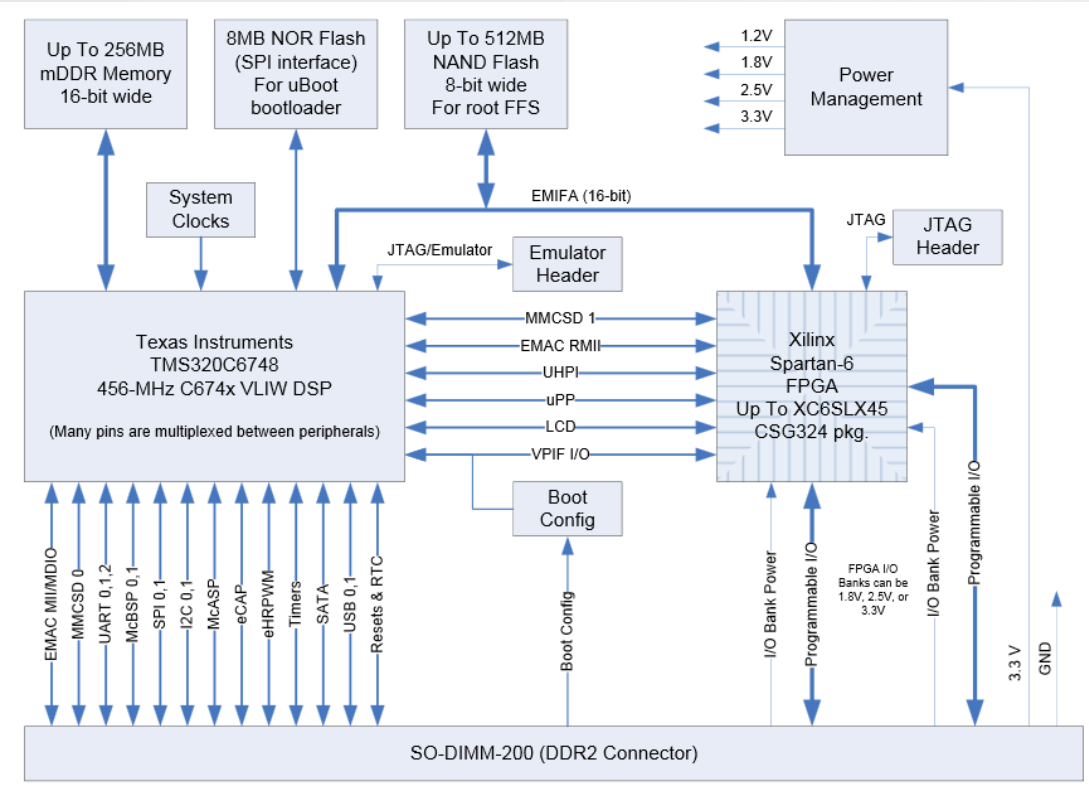


(b) $\mu = 1 \times 10^{-5}$の場合

Digital filter implementation

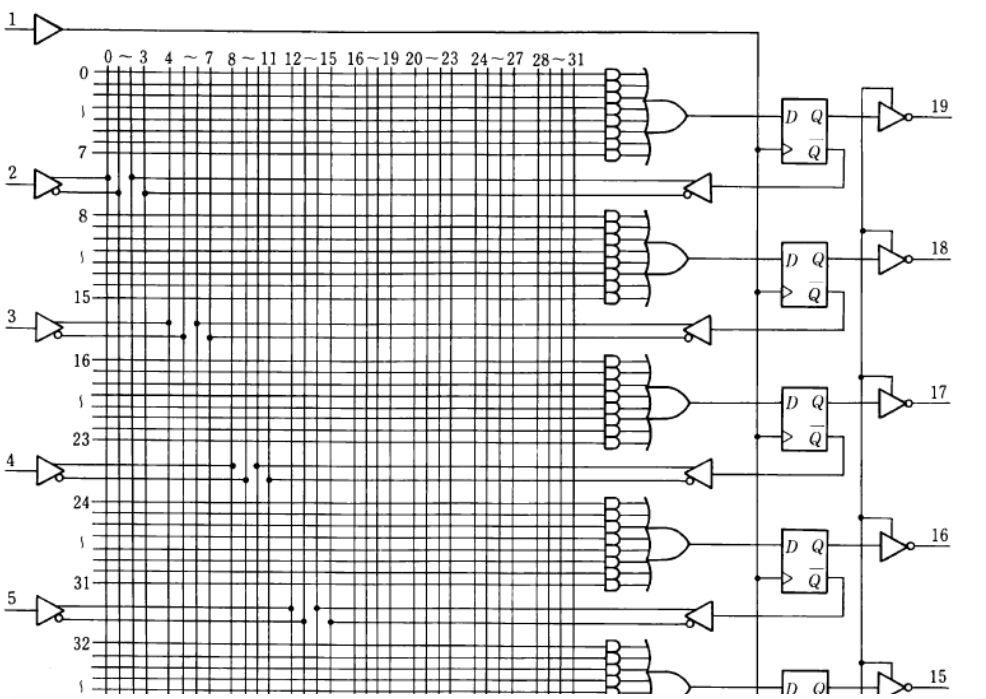
Digital signal processing (DSP) board



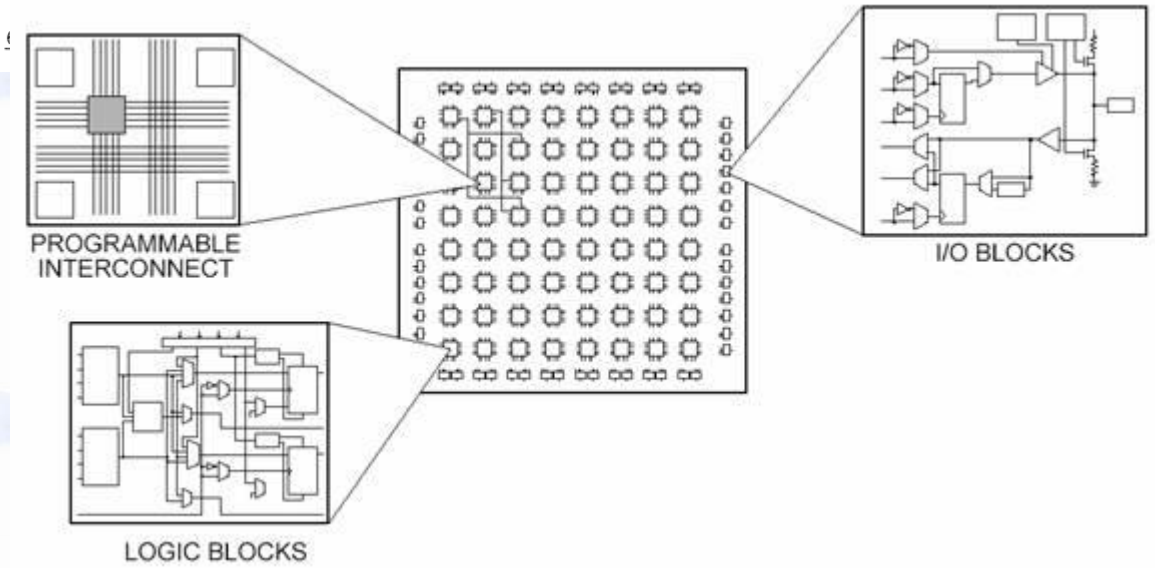


PLD/FPGA with HDL

Example of programmable logic device (PLD) circuit



Example of field-programmable gate array (FPGA) circuit



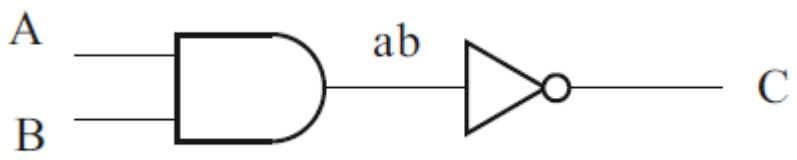
FPGA ∈ PLD

Hardware description language, HDL

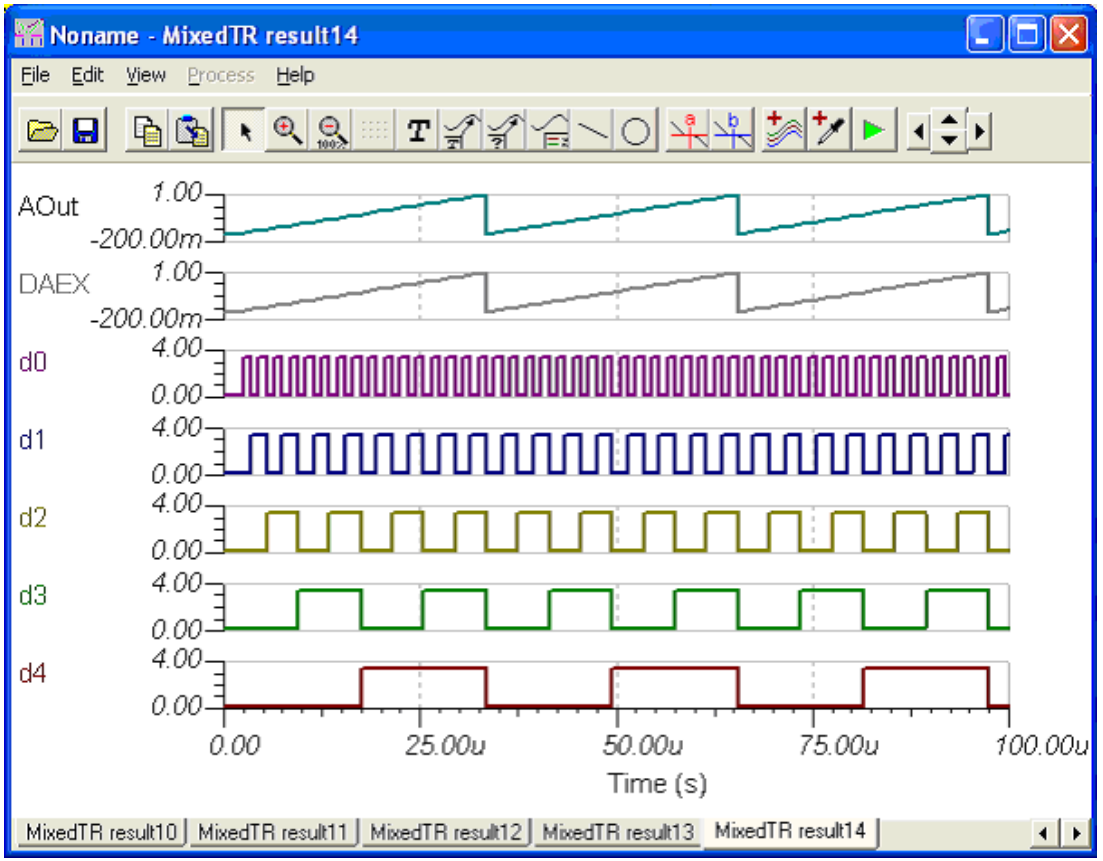
```
-- Library declaration --------------
library IEEE;
use IEEE, STD_LOGIC_1164.ALL;
-- Entity declaration ---------------
entity NAND_CIRCUIT is
port(
A : in std_logic;
B : in std_logic;
C : out std_logc
);
end NAND_CIRCUIT;
-- Architecture declaration ----------
architecture RTL of NAND_CIRCUIT is
signal ab : std_logic;
begin
ab <= A and B;
C  <= not ab;
end RTL;
```

RTL: register transfer level

Cf. SPICE

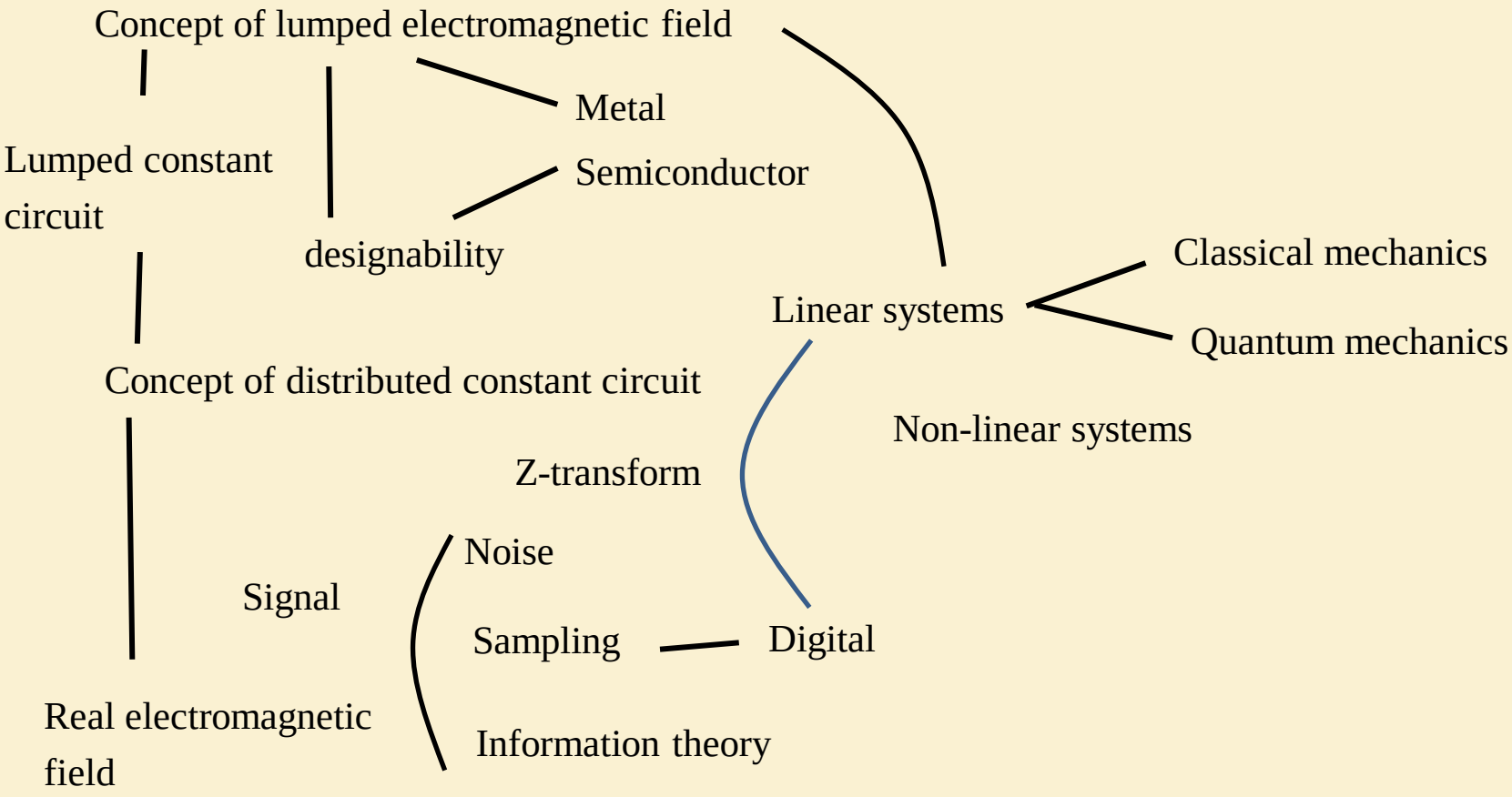


Mixed circuit simulation



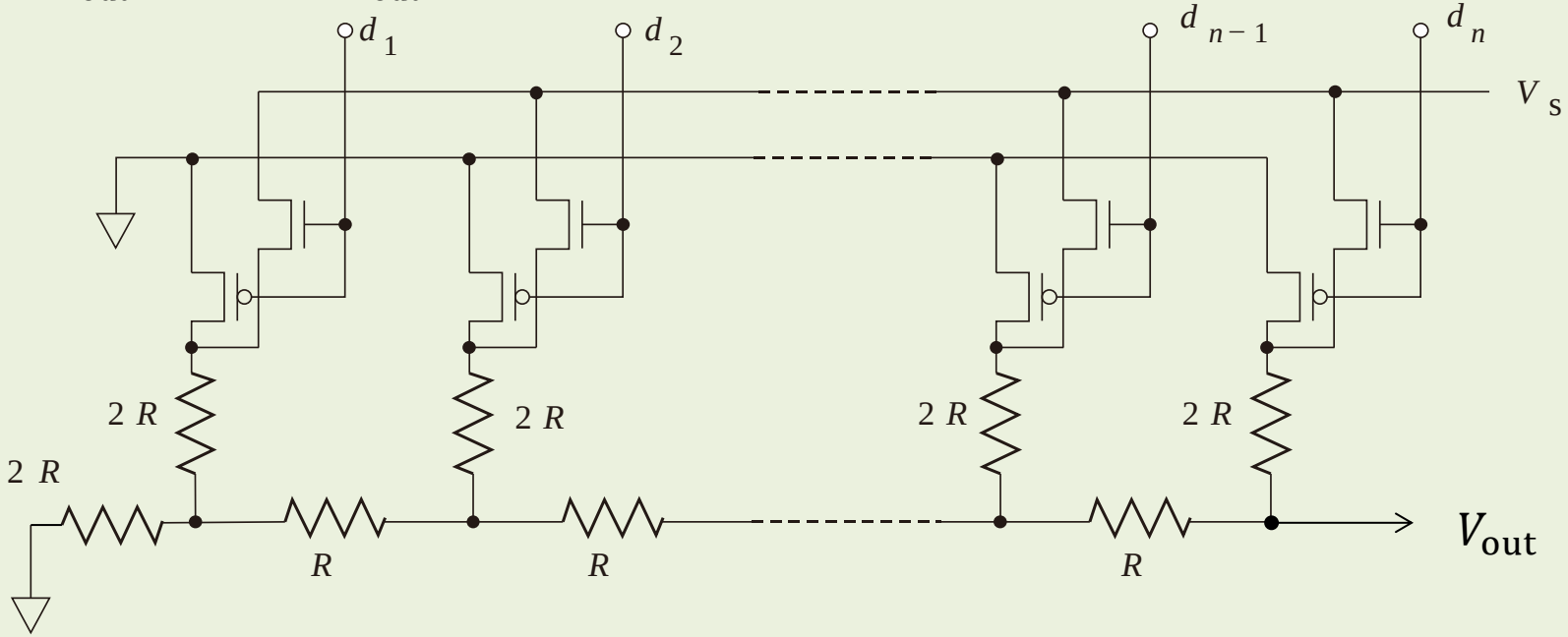
Overview

Electric Circuits: Treasury of Languages and Concepts



電子回路論レポート問題: 1. DA変換回路

(1) 次の図のような抵抗ラダー型DA変換回路を考える．講義で扱ったものと端の処理だけが違っている．この回路に2進数列$\{d_k\}(k = 1,..,n)$が入力されたとき，出力電圧V_{out}を求めよ． V_{out}は，高入力インピダンスアンプで受けるものとする．



(2) 手元に，$\{R_0/2^k\}$ (k =0, …, n)の抵抗値列を持つ抵抗，抵抗値R_{f} の抵抗，OPアンプ，電圧V_{S}の標準電源，n +1個のnチャネルMOSスイッチ，同じくn +1個のpチャネルMOSスイッチがある．これらを使って，2進数列$\{d_k\}$が入力された時に

$$V_{\text{out}} = -V_{\text{s}}\frac{R_{\text{f}}}{R_0}\sum_{k=0}^{n} d_k 2^k$$

を出力するDA変換器回路を考えなさい．

電子回路レポート問題：1. DA変換回路

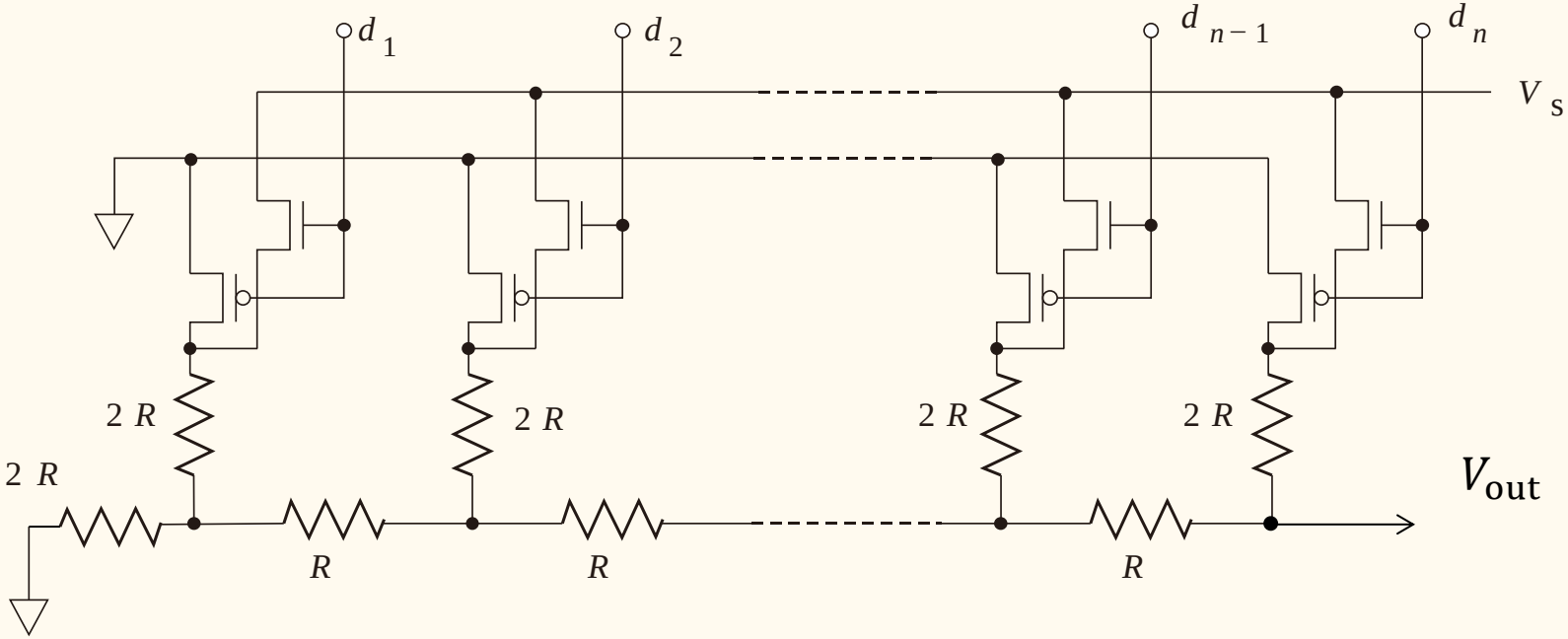
(3) (2) と同様，に手元に，$\{2^k C_0\}$ (k =0, …, n)の抵抗値列を持つキャパシタ，電圧V_Sの標準電源，n +1個のnチャネルMOSスイッチ，同じくn +1個のpチャネルMOSスイッチがある．これらを使って，2進数列$\{d_k\}$が入力された時に

$$V_{\mathrm{out}} = \frac{V_{\mathrm{s}}}{2^{n+1} - 1} \sum_{k=0}^{n} d_k 2^k$$

という出力が得られるようなDA変換回路を考えなさい．ただし，出力は入力インピダンスが高くバイアス電流が無視できるような増幅器で受けることとする．

Problems for the final report: 1. DA conversion circuits

(1) Let us consider the following resistance ladder DA conversion circuit. The right end is a bit different from the one we treated in the lecture. Calculate the output voltage V_{out} for the input $\{d_k\}$ $(k = 1, \cdots, n)$.



(2) We have resistors with values $\{R_0/2^k\}$ $(k = 0, \cdots, n)$, and R_{f}, an OP amp., a standard voltage source of the voltage V_{S}, $n + 1$ n-channel MOS switches, $n + 1$ p-channel MOS switches. With these components, design a DA conversion circuit which has the output

$$V_{\text{out}} = -V_{\text{S}} \frac{R_{\text{f}}}{R_0} \sum_{k=0}^{n} d_k 2^k$$

for the binary input $\{d_k\}$.

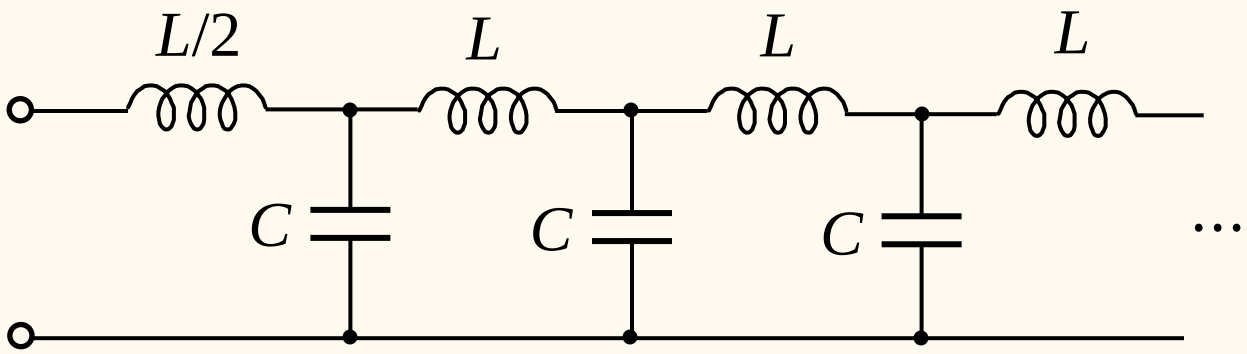
Problems for the final report: 1. DA conversion circuits

(3) We have capacitors with values $\{2^k C_0\}$ $(k = 0, \cdots, n)$, a standard voltage source of the voltage V_S, $n+1$ n-channel MOS switches, $n+1$ p-channel MOS switches. With these components, design a DA convertor circuit which has the output

$$V_{\text{out}} = \frac{V_S}{2^{n+1} - 1} \sum_{k=0}^{n} d_k 2^k$$

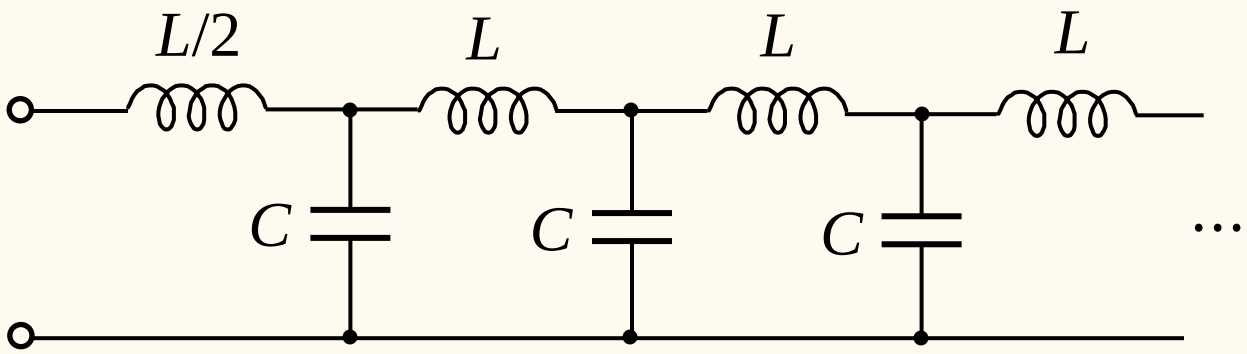
for the binary input $\{d_k\}$.

電子回路論レポート問題：2. 分布定数回路



上図のように，端のインダクタンス$L/2$を除いてLとCが無限に繰り返す回路がある．この回路の，周波数軸上での透過域と減衰域を求めよ．また，左の端子から見たインピーダンスの周波数特性(周波数ωに対するインピーダンス)を求めよ．

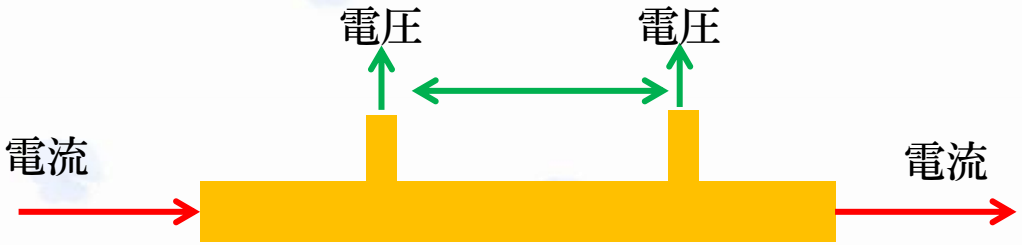
Problems for the final report: 2. Distributed constant circuit



Consider the above circuit with L, C infinite repetition to the right and the inductor $L/2$ at the left end. Obtain the transmission range and the attenuation range in the frequency domain. And what is the total impedance from the left end for the frequency ω.

電子回路論レポート問題：3. OPアンプ回路

次のような回路部品がある．
高精度OPアンプ ・・・　4個
定電圧ダイオード (逆方向に電圧を印加するとツェナートンネルにより一定電圧を発生する)　2.5V ・・・　1個
これらを使って，低温で試料の電気抵抗を測定するための回路を構成しなさい．
試料は下の図のように，電流端子，電圧端子が別に出た構造をしている．

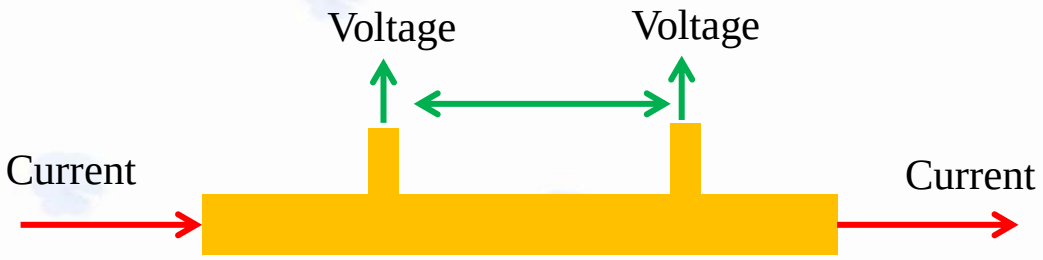


ただし，

(a) 抵抗，キャパシタ，インダクタの類の受動素子は適当に追加してよい．
(b) OPアンプの電源を供給するためのトラッキング電源は準備されているものとする．
(c) 測定抵抗の範囲は100Ω～10kΩで，接触抵抗を含めて50kΩ以内である．
(d) OPアンプのオフセット電圧，バイアス電流は無視できるとする．従ってオフセット調整回路を入れる必要はない．

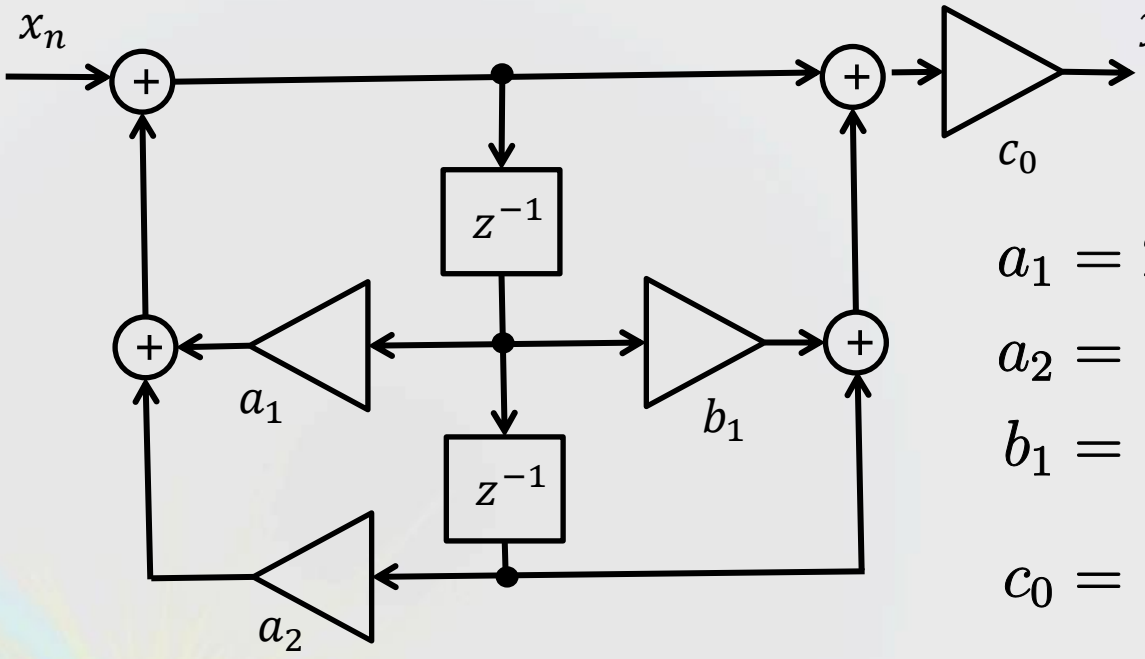
Problems for the final report: 3. OP amp. circuit

We have the following components:
4 high precision operational amplifiers,
1 high precision Zener tunnel diode with the constant voltage 2.5V (this diode provide precise 2.5V for the reverse bias).
With these components, design a circuit to measure the electric resistance of a sample at low temperatures. The shape of the sample is shown below:



(a) You can add any passive elements (resistors, capacitors, inductors).
(b) The power supply for the OP amps. is ready.
(c) The sample resistance range is from 100Ω to 10kΩ, lower than 50kΩ including the contact resistance.
(d) The offset voltages, the bias currents of the OP amps. can be ignored. No need for the offset cancellation circuit.

電子回路論レポート問題：4. ディジタル・フィルター

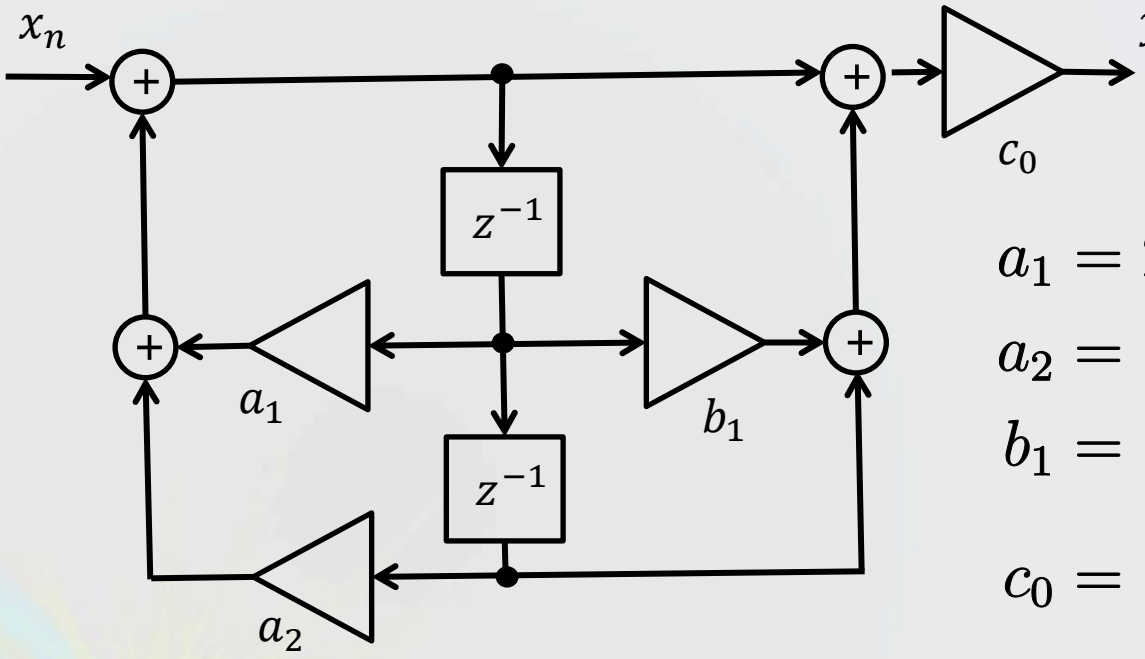


$$a_1 = 2\exp(-\pi g_0 \tau)\cos(2\pi f_0 \tau)$$
$$a_2 = -\exp(-2\pi g_0 \tau)$$
$$b_1 = -2\cos(2\pi f_0 \tau)$$
$$c_0 = \frac{1 - a_1 - a_2}{2 + b_1}$$

(1) 上のブロックダイアグラムから，出力y_n, y_{n-1}, y_{n-2}と入力x_n, x_{n-1}, x_{n-2}との関係式を示せ．

(2) 係数a_1， a_2， b_1， c_0 が右上のような関係を満たすとき，このフィルターはどのような周波数特性を示すか．ただし，$g_0 < f_0 < f_s/2$ (サンプリング周波数)を満たすとする．($20g_0 = 10f_0 = f_s$ としてグラフを描いてみよ．)

Problems for the final report: 4. Digital filter

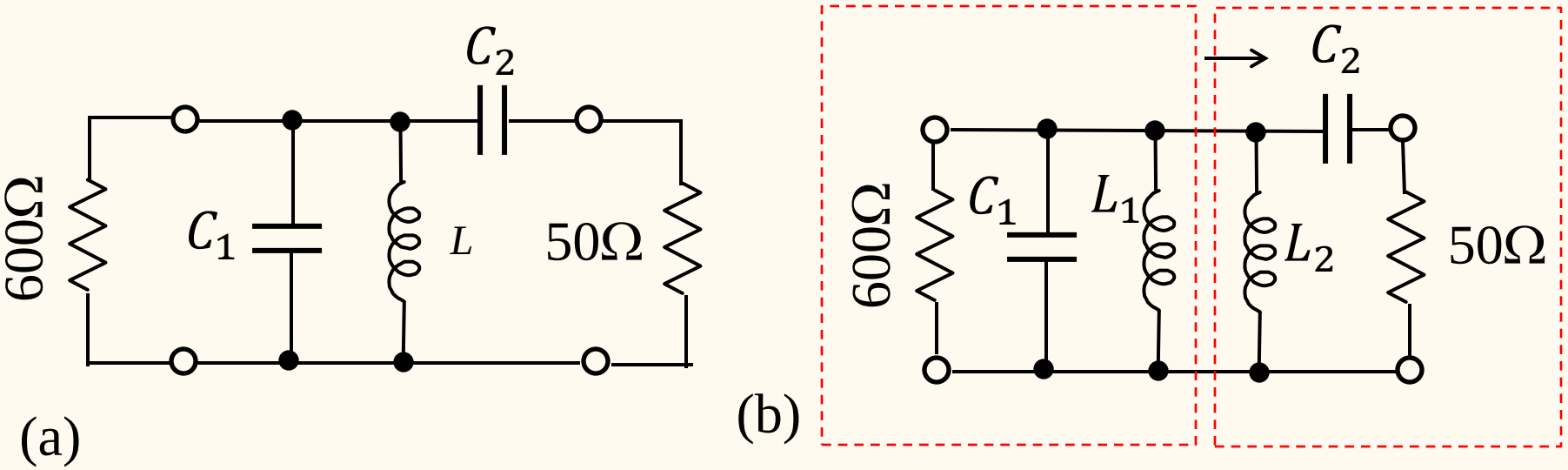


$$a_1 = 2\exp(-\pi g_0 \tau)\cos(2\pi f_0 \tau)$$
$$a_2 = -\exp(-2\pi g_0 \tau)$$
$$b_1 = -2\cos(2\pi f_0 \tau)$$
$$c_0 = \frac{1 - a_1 - a_2}{2 + b_1}$$

(1) From the above diagram, write down the relation between the output y_n, y_{n-1}, y_{n-2} and the input x_n, x_{n-1}, x_{n-2}.

(2) When the coefficients a_1, a_2, b_1, c_0 satisfy the above relations, obtain the frequency characteristics of this filter. Draw a rough sketch of the graph for $20g_0 = 10f_0 = f_s$.

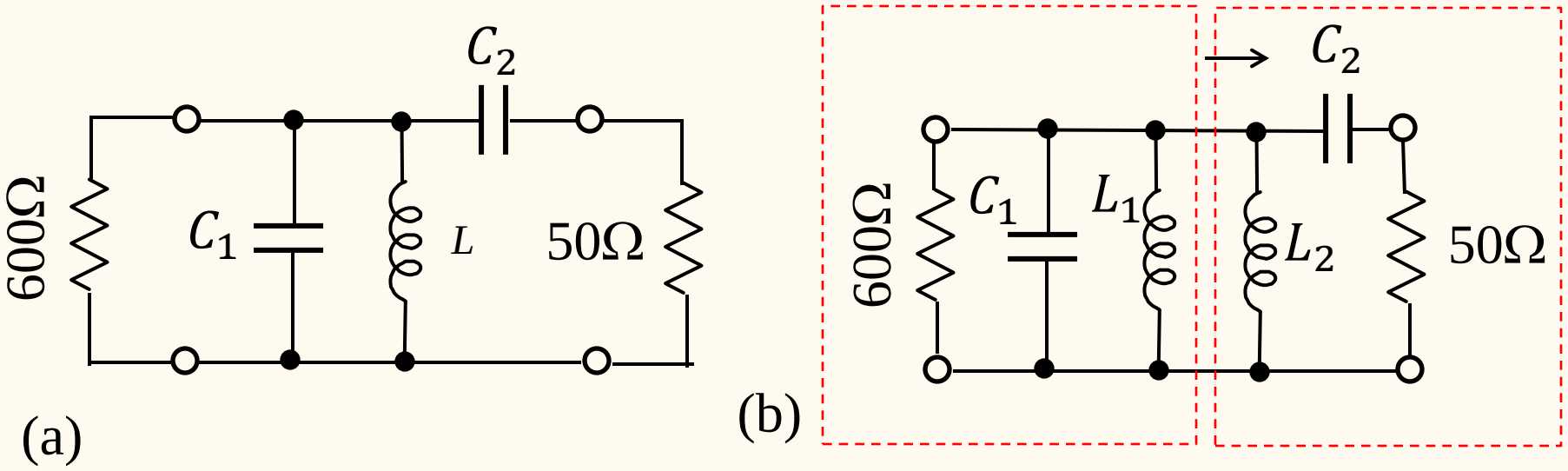
電子回路論レポート問題：5. インピーダンスマッチ



FM受信機のプリアンプをFETで作ったところ，出力インピーダンスが600Ωになった．受信機の入力インピーダンスは50Ωなので，インピーダンスマッチを取る必要がある．中心周波数を85MHz，有効周波数幅を10MHz，として(a)のような回路でマッチを取ると，回路定数C_1, C_2, Lはどうなるか．有効数字3桁で答えよ．

(ヒント) (b)のようにインダクタンスを２つに分割し，左の共鳴回路で85MHz，10MHz幅に同調させる．この後，左右のインピーダンスが一致するように定数を求める．

Problems for the final report: 5. Impedance matching

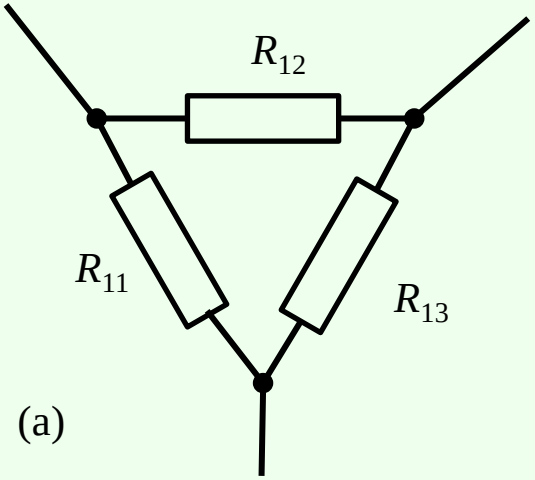


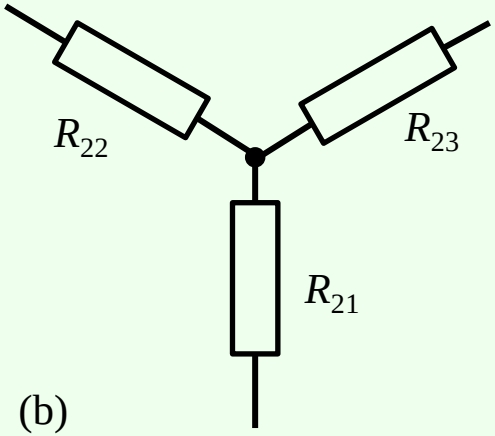
A preamplifier with FETs for an FM receiver has the output impedance of 600Ω. The FM receiver has the input impedance of 50Ω and we need to make impedance matching. The central frequency is 85MHz, the effective with of amplification is 10MHz. Obtain C_1, C_2, L in the matching circuit with 3 digits significant figures.

(hint) Express L with a parallel of L_1 and L_2 as shown in (b). The left resonance circuit should be tuned to 85MHz, width10MHz. Then the left and the right circuit should be impedance matched.

電子回路論レポート問題：6. 回路網

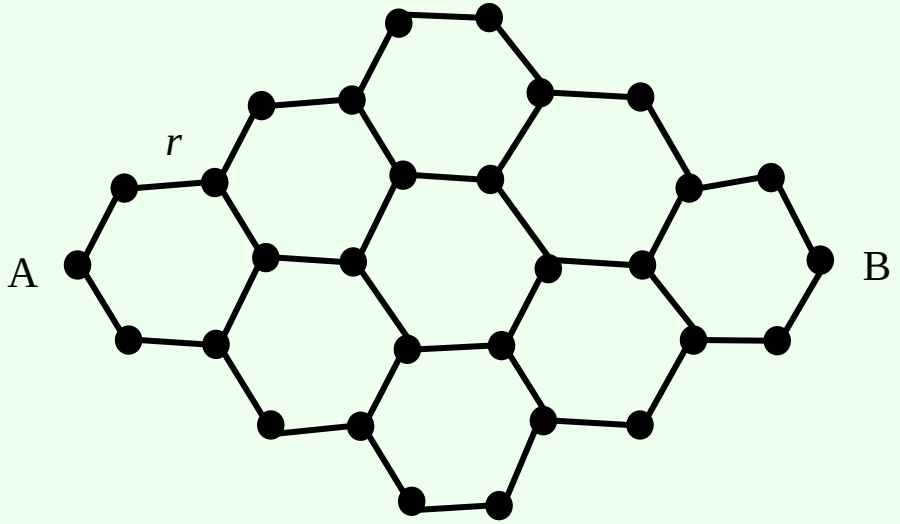
(1) (a)のような△結線網と,(b)のようなY結線網とが外部に対して全く等価になるためには，R_{ij}の間にどのような関係があればよいか．(Δ-Y変換)





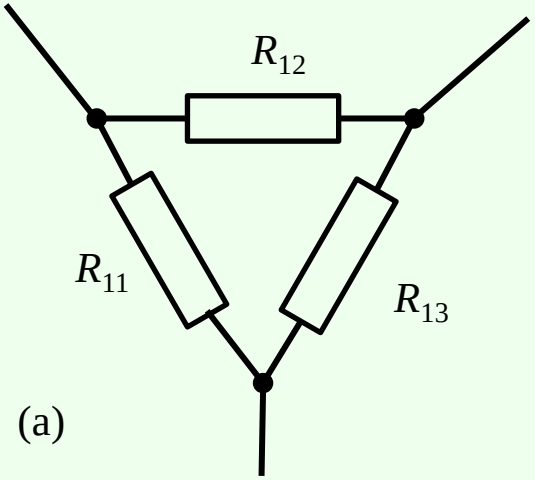
(2) 右図のようにすべて同じ抵抗値 r の抵抗で対称な蜂の巣状格子を作ると，A-B間の電気抵抗はいくらになるか．

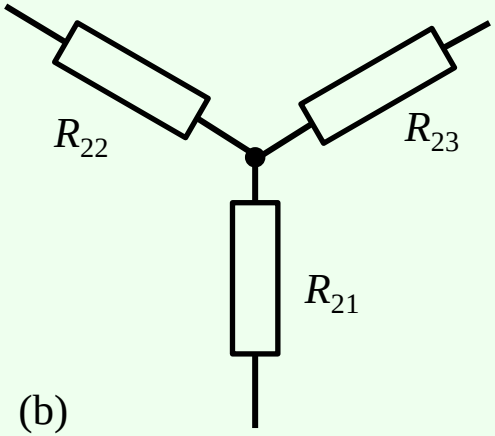
(ヒント) 回路の対称性を考え，(1)のΔ-Y変換を適用するとよい．



Problems for the final report: 6. Resistor network

(1) Obtain the sufficient condition on R_{ij} for the circuits (a) and (b) to be equivalent.
(Δ-Y transform)





(2) Calculate the resistance between A and B, which are connected with the honeycomb of resistances r as shown in the right figure.
(hint) Consider the symmetry of the circuit and apply Δ-Y transform.